

Model Name: KML50 DIS
PCB NO: LA-4595PR04
BOM P/N: DA80000DR00

Half Penny Bridge 15.4

Compal Confidential

Schematic Document

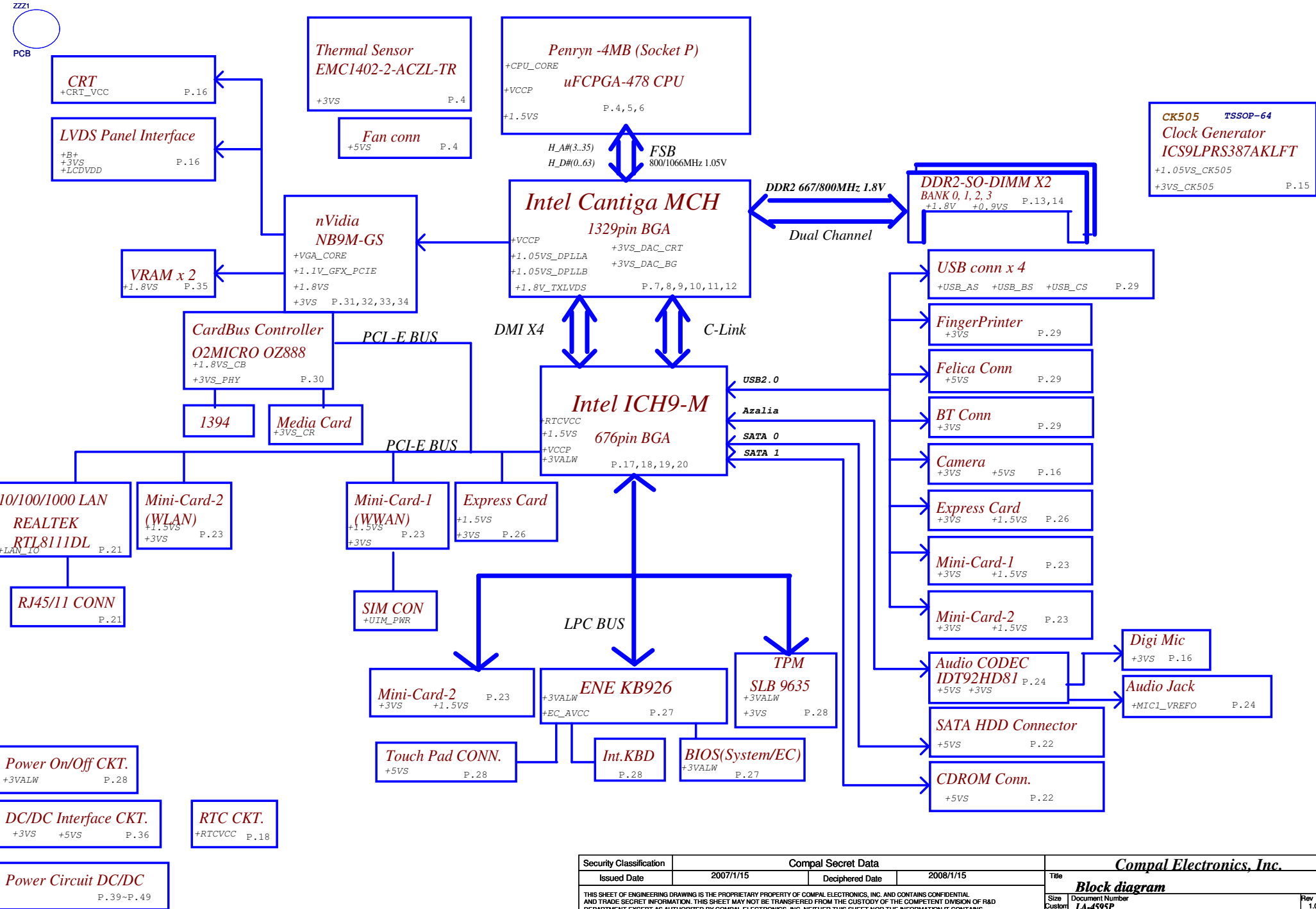
Cantiga + ICH9

2009 / 02 / 17 Rev:1.0 (A00)

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Half Penny Bridge 15.4 DIS

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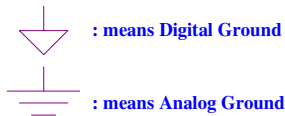


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power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1V_GFX_PCIEP
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3 TOP
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3 BOT
	9	JMINI1-WWAN
	10	JUSBP4
11	NA	

Symbol Note :



@ : means just reserve , no build
CON@ : means ME connectors
TPM@ : means TPM function

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

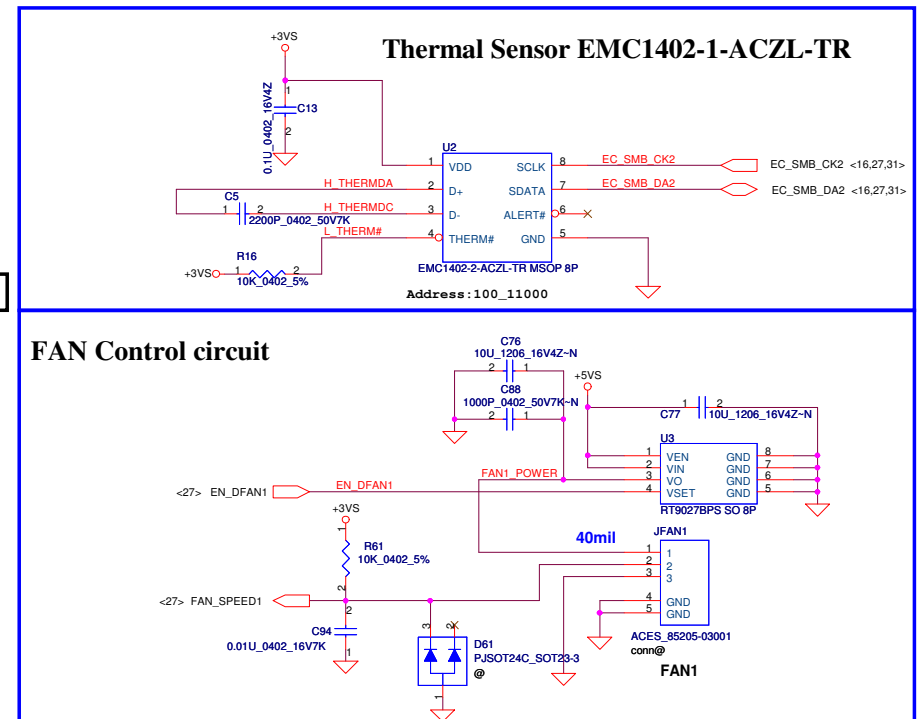
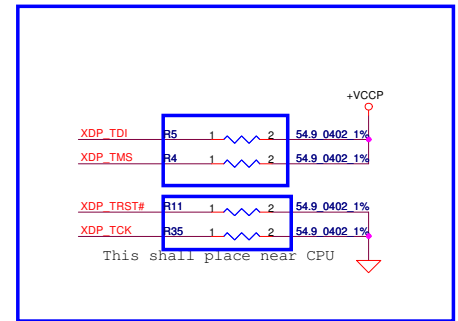
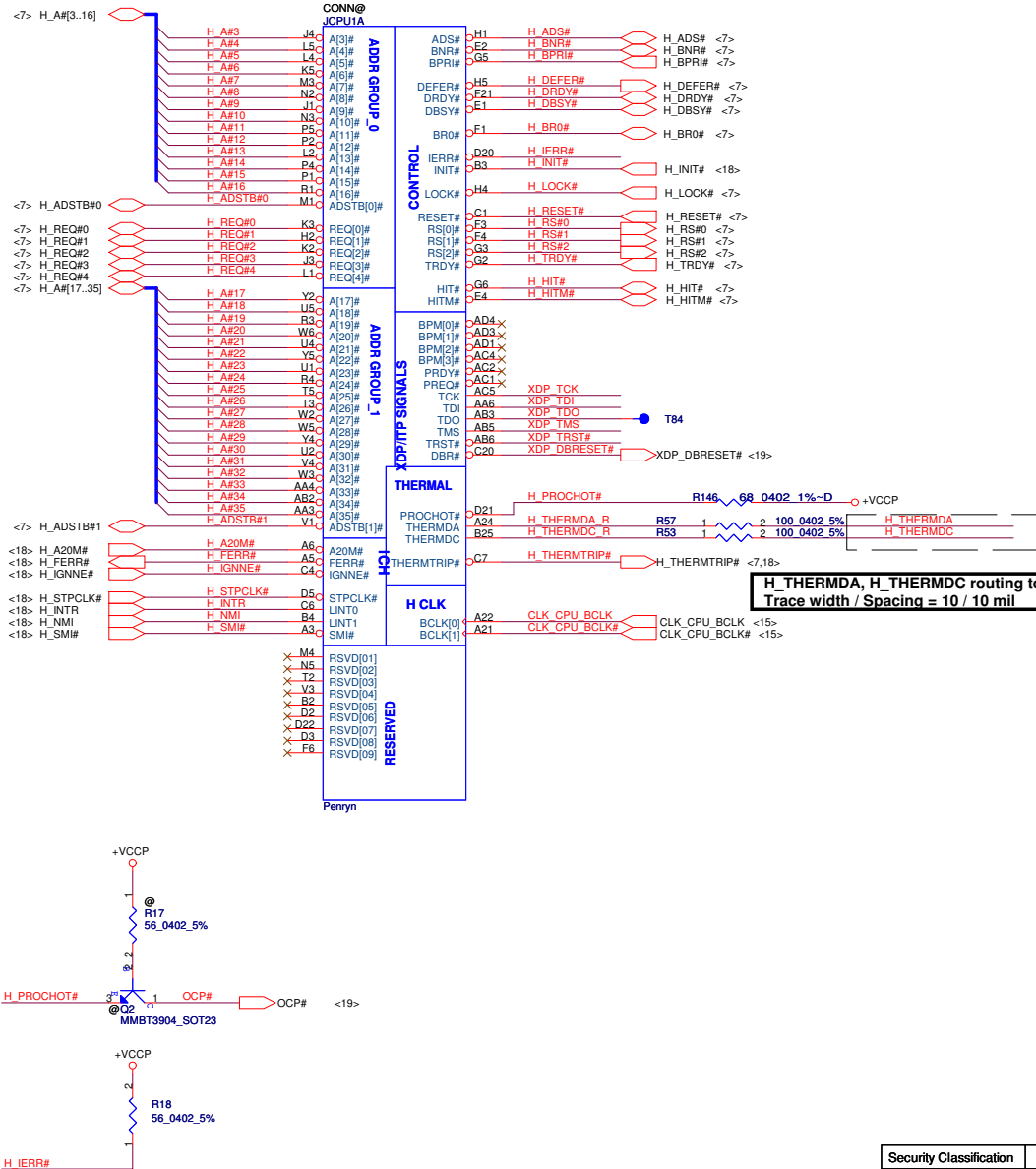
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

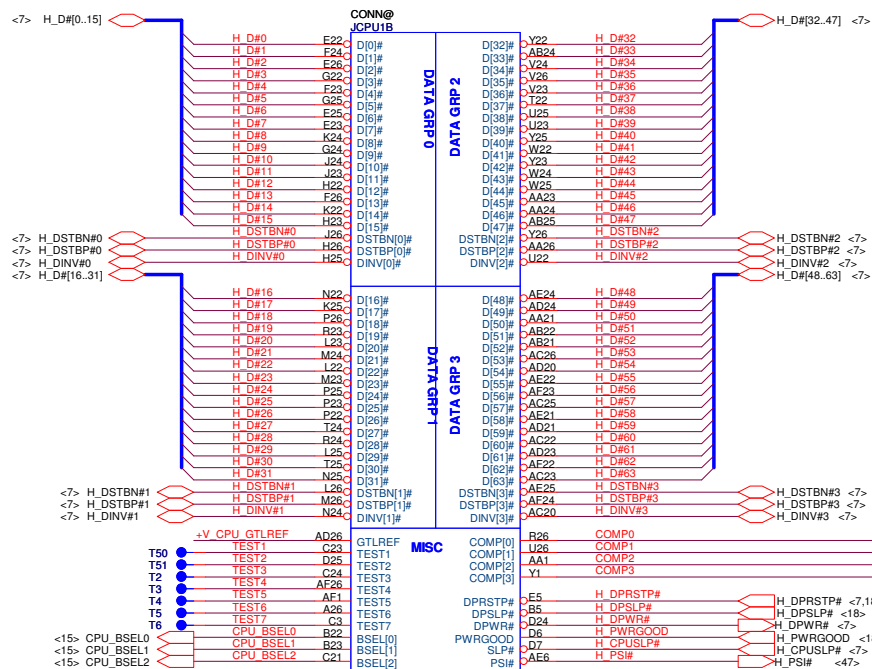
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
LED panel	58	01011000

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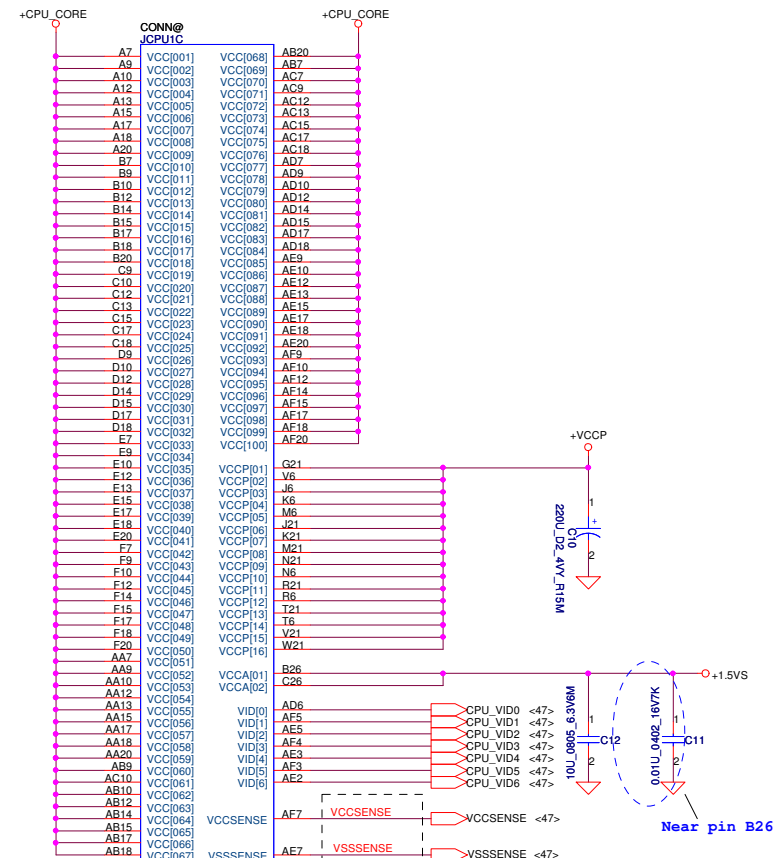
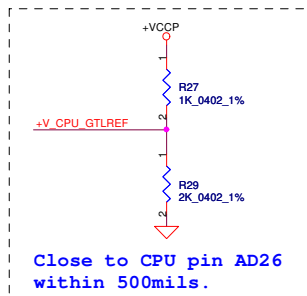


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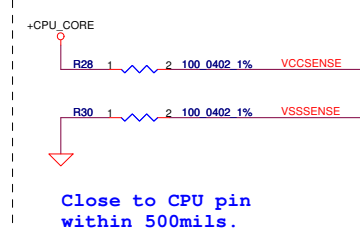


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

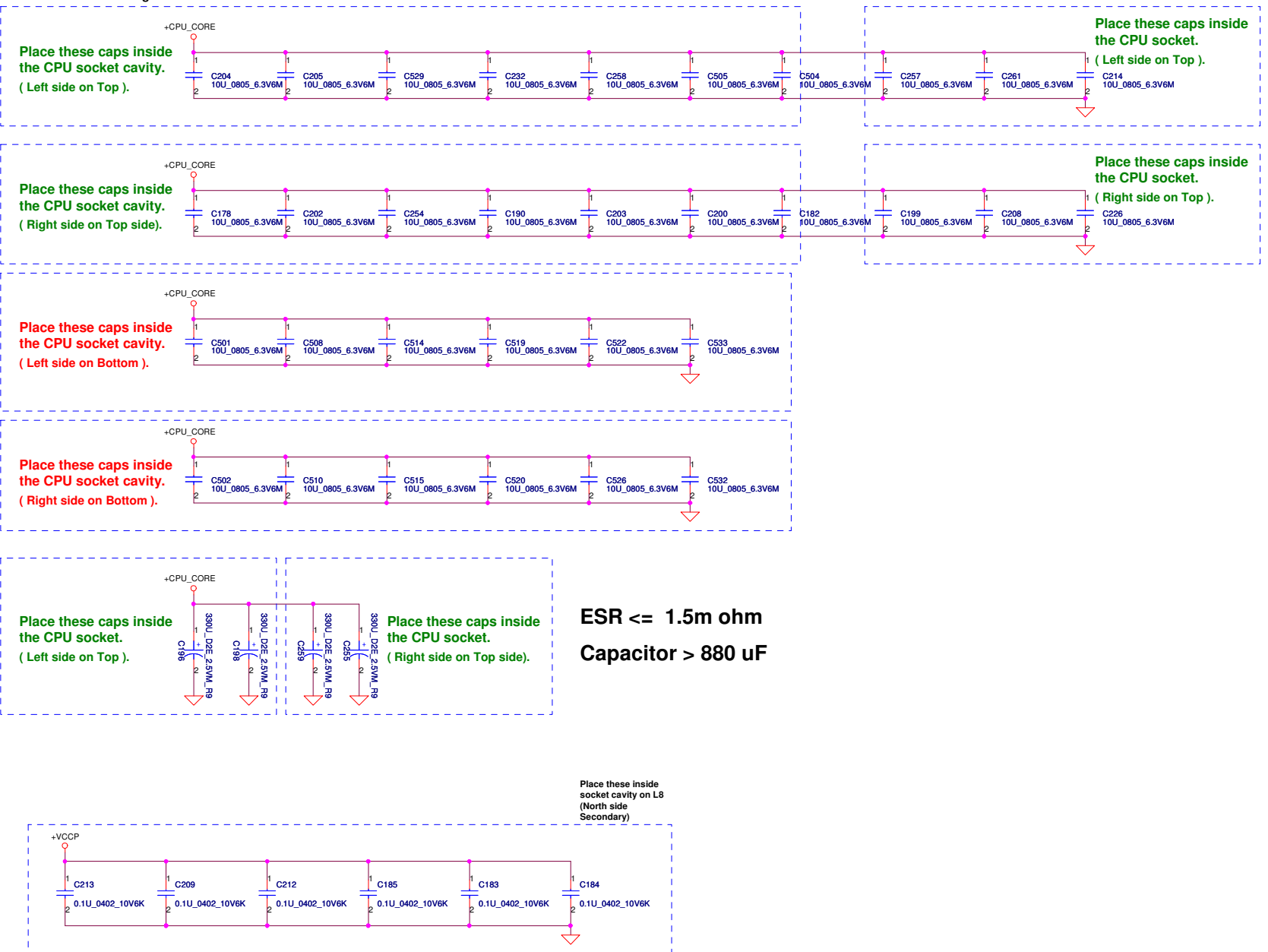
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4



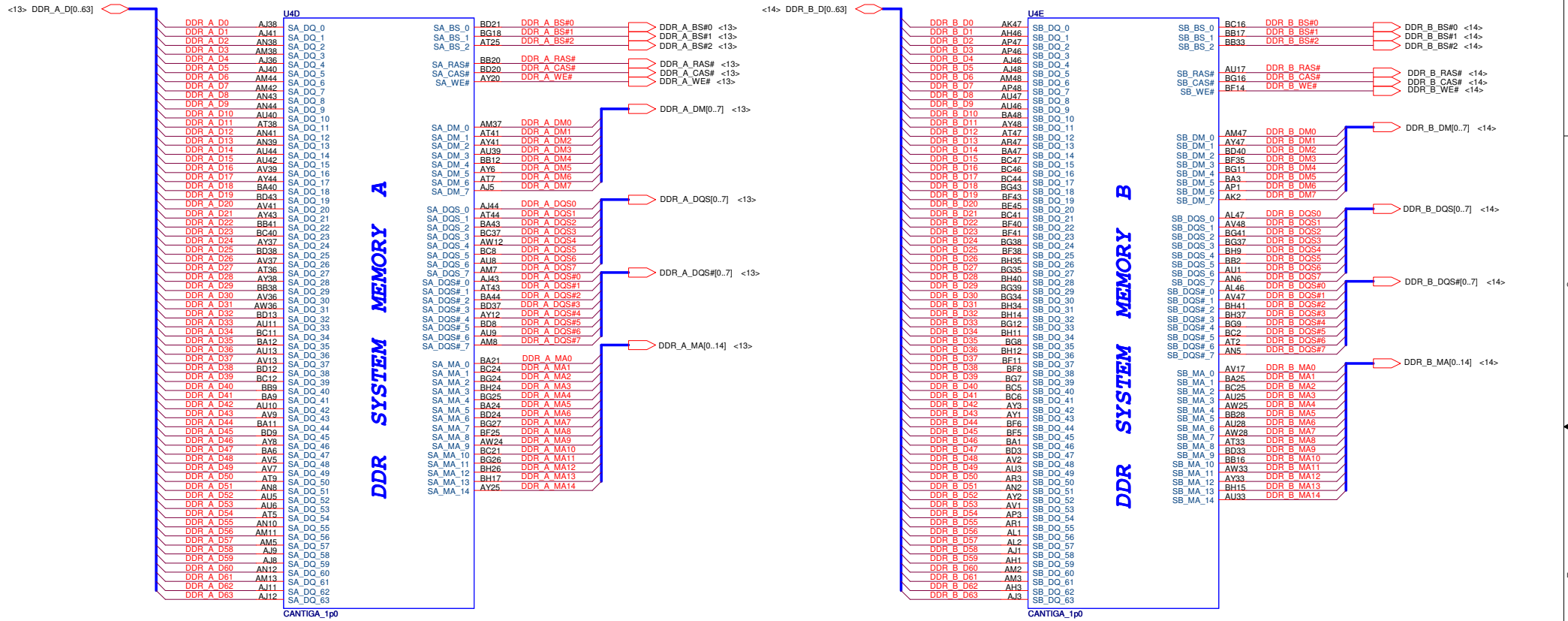
For 8 layer condition Length match within 25 mils. Z0=27.4 ohm The trace width/space/other is 20/7/25.



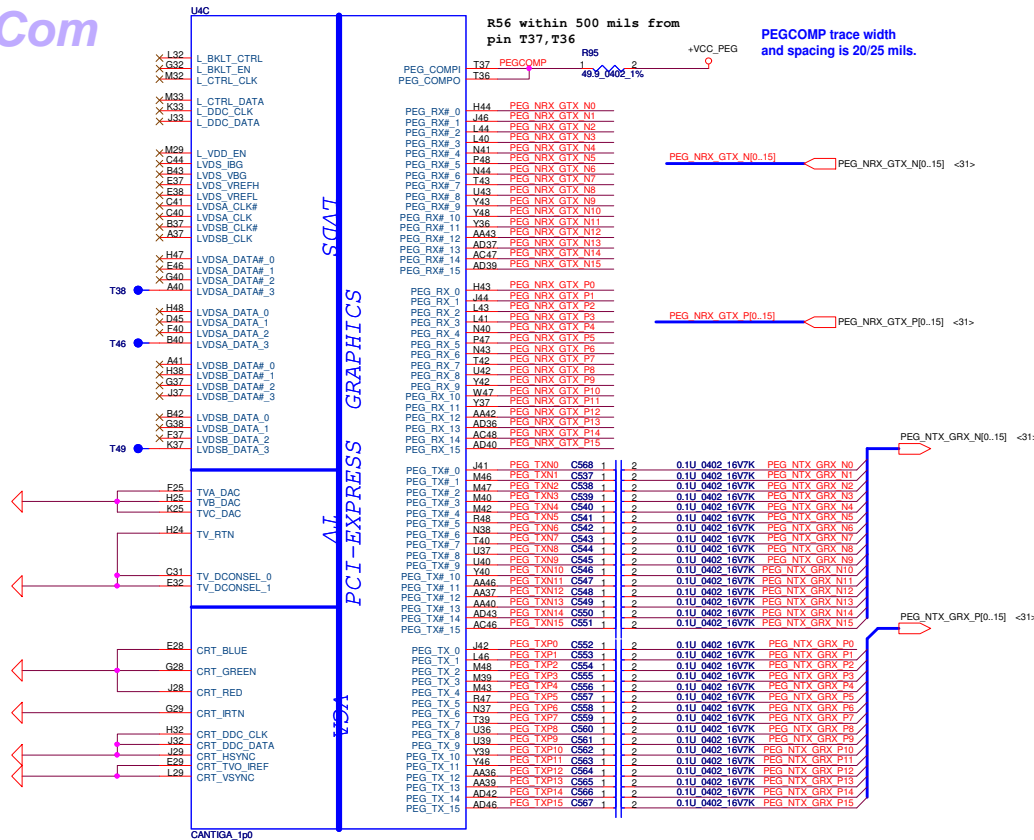
CONN@		CPUID	
A4	VSS[001]	P6	VSS[002]
A8	VSS[002]	P21	VSS[003]
A11	VSS[003]	P24	VSS[004]
A14	VSS[004]	R5	VSS[005]
A19	VSS[005]	R22	VSS[006]
A23	VSS[006]	R25	VSS[007]
A2	VSS[007]	T4	VSS[008]
B6	VSS[008]	T23	VSS[009]
B8	VSS[009]	T26	VSS[010]
B11	VSS[010]	U3	VSS[011]
B13	VSS[011]	U6	VSS[012]
B16	VSS[012]	U21	VSS[013]
B19	VSS[013]	U24	VSS[014]
B21	VSS[014]	V2	VSS[015]
B24	VSS[015]	V5	VSS[016]
C5	VSS[016]	V22	VSS[017]
C8	VSS[017]	V25	VSS[018]
C11	VSS[018]	W1	VSS[019]
C14	VSS[019]	W23	VSS[020]
C16	VSS[020]	W26	VSS[021]
C19	VSS[021]	Y3	VSS[022]
C22	VSS[022]	Y6	VSS[023]
C25	VSS[023]	Y21	VSS[024]
D1	VSS[024]	Y24	VSS[025]
D4	VSS[025]	AA2	VSS[026]
D8	VSS[026]	AA5	VSS[027]
D11	VSS[027]	AA8	VSS[028]
D13	VSS[028]	AA11	VSS[029]
D16	VSS[029]	AA14	VSS[030]
D19	VSS[030]	AA16	VSS[031]
D23	VSS[031]	AA19	VSS[032]
D26	VSS[032]	AA22	VSS[033]
E3	VSS[033]	AA25	VSS[034]
E6	VSS[034]	AB1	VSS[035]
E8	VSS[035]	AB4	VSS[036]
E11	VSS[036]	AB8	VSS[037]
E14	VSS[037]	AB11	VSS[038]
E16	VSS[038]	AB13	VSS[039]
E19	VSS[039]	AB16	VSS[040]
E21	VSS[040]	AB19	VSS[041]
E24	VSS[041]	AB23	VSS[042]
F5	VSS[042]	AB26	VSS[043]
F8	VSS[043]	AC3	VSS[044]
F11	VSS[044]	AC6	VSS[045]
F13	VSS[045]	AC8	VSS[046]
F16	VSS[046]	AC11	VSS[047]
F19	VSS[047]	AC14	VSS[048]
F22	VSS[048]	AC16	VSS[049]
F25	VSS[049]	AC19	VSS[050]
G4	VSS[050]	AC21	VSS[051]
G11	VSS[051]	AC24	VSS[052]
G23	VSS[052]	AD2	VSS[053]
G26	VSS[053]	AD5	VSS[054]
H3	VSS[054]	AD8	VSS[055]
H6	VSS[055]	AD11	VSS[056]
H21	VSS[056]	AD13	VSS[057]
H24	VSS[057]	AD16	VSS[058]
J2	VSS[058]	AD19	VSS[059]
J5	VSS[059]	AD22	VSS[060]
J22	VSS[060]	AD25	VSS[061]
J25	VSS[061]	AE1	VSS[062]
K1	VSS[062]	AE4	VSS[063]
K4	VSS[063]	AE8	VSS[064]
K23	VSS[064]	AE11	VSS[065]
K26	VSS[065]	AE14	VSS[066]
L3	VSS[066]	AE16	VSS[067]
L6	VSS[067]	AE19	VSS[068]
L21	VSS[068]	AE23	VSS[069]
L24	VSS[069]	AE26	VSS[070]
M2	VSS[070]	A2	VSS[071]
M5	VSS[071]	AF6	VSS[072]
M22	VSS[072]	AF8	VSS[073]
M25	VSS[073]	AF11	VSS[074]
N1	VSS[074]	AF13	VSS[075]
N4	VSS[075]	AF16	VSS[076]
N23	VSS[076]	AF19	VSS[077]
N26	VSS[077]	AF21	VSS[078]
P3	VSS[078]	A25	VSS[079]
	VSS[079]	AF25	VSS[080]
	VSS[080]		VSS[081]
	VSS[081]		VSS[082]
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	VSS[156]		VSS[157]
	VSS[157]		VSS[158]
	VSS[158]		VSS[159]
	VSS[159]		VSS[160]
	VSS[160]		VSS[161]
	VSS[161]		VSS[162]
	VSS[162]		VSS[163]



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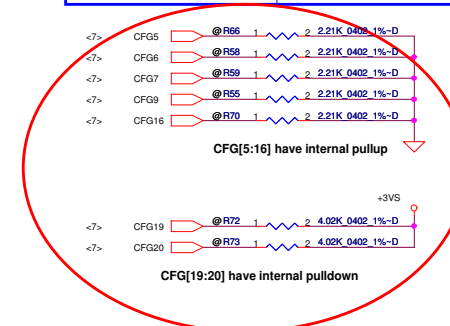


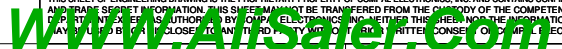
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Strap Pin Table

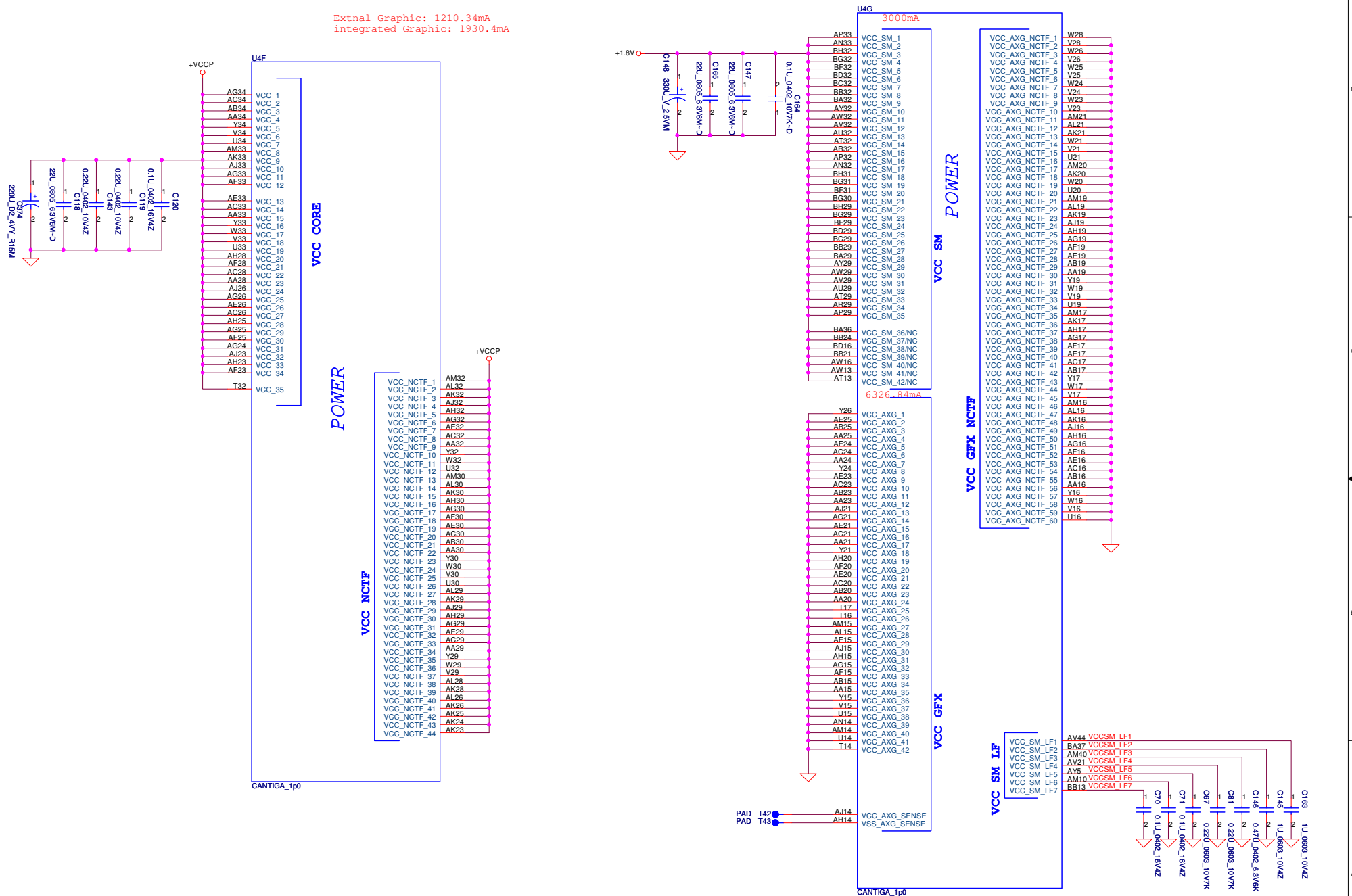
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chipr suite with no confidentiality 1 = (TLS)chipr suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



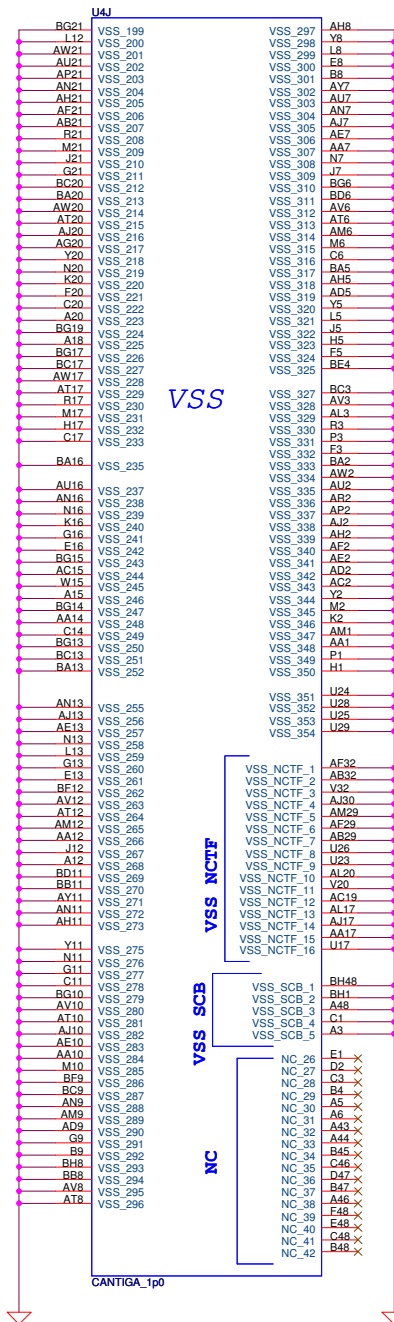
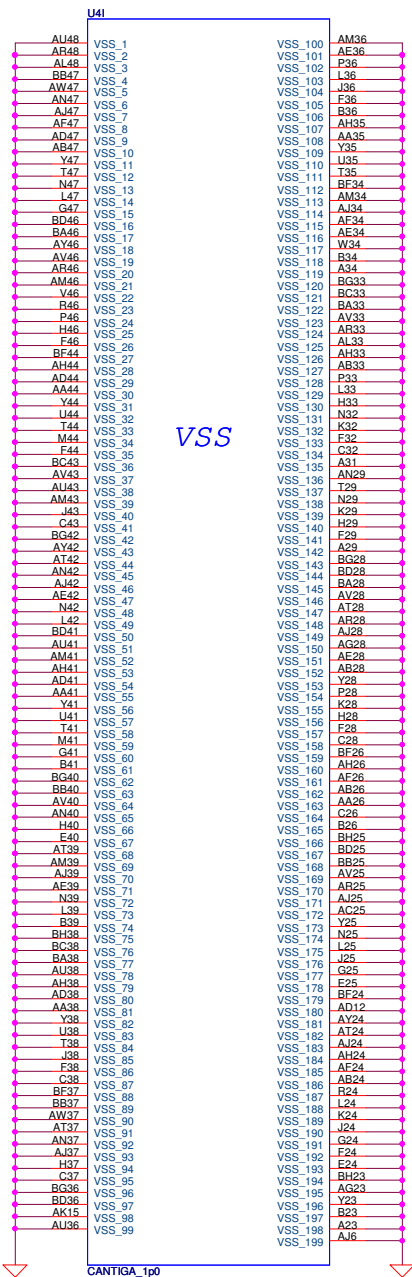


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Extlnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



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VSS NCTF

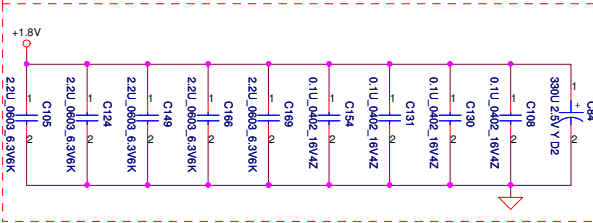
VSS SCB

NC

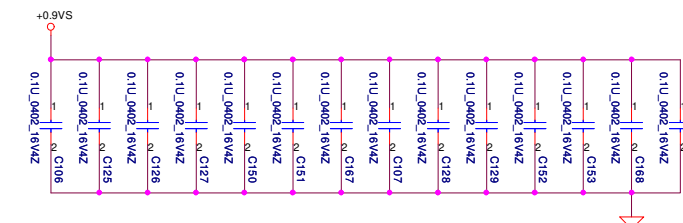
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<8> DDR_A_DQS[0..7]
 <8> DDR_A_D[0..63]
 <8> DDR_A_DM[0..7]
 <8> DDR_A_DQS[0..7]
 <8> DDR_A_MA[0..13]

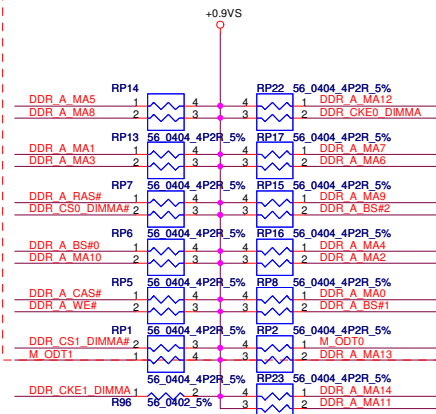
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



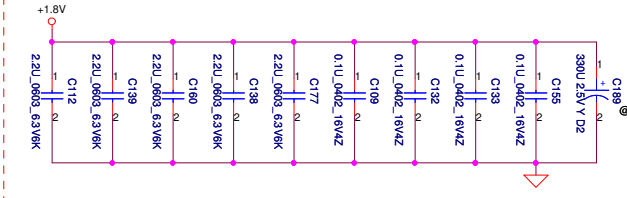
Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



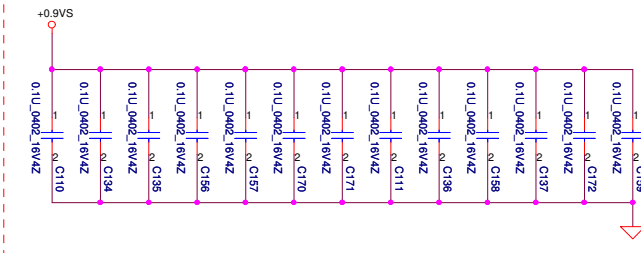
SO-DIMM A
REVERSE
Bottom side

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								2008/1/15			
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								DDR2 SO-DIMM I			
								Document Number			
								LA-4595P			
								Rev			
								1.0			
								Date			
								Tuesday, February 17, 2009			
								Sheet 13 of 49			

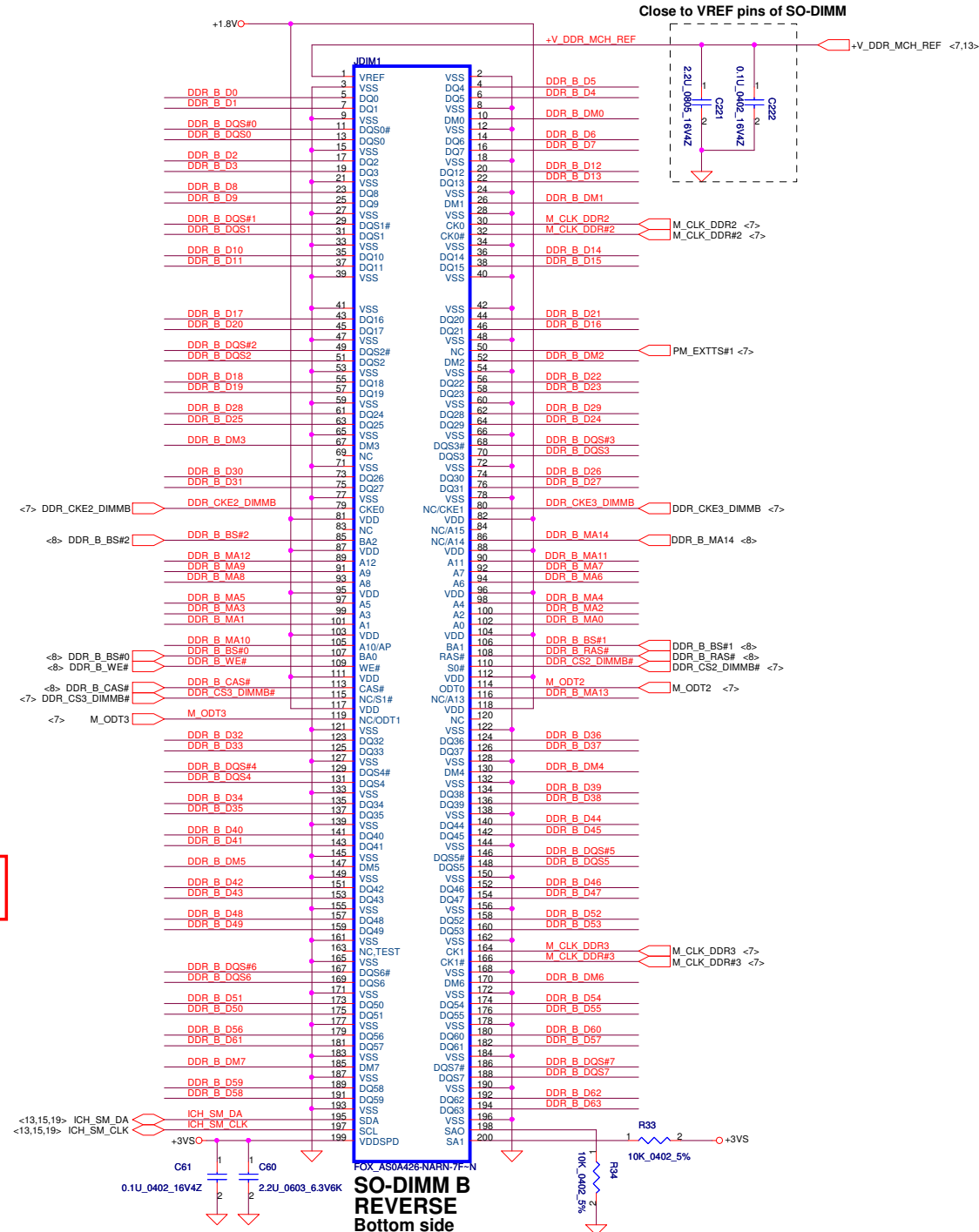
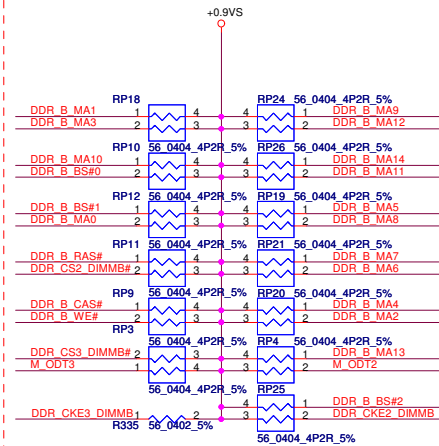
Layout Note:
Place near JDIM2



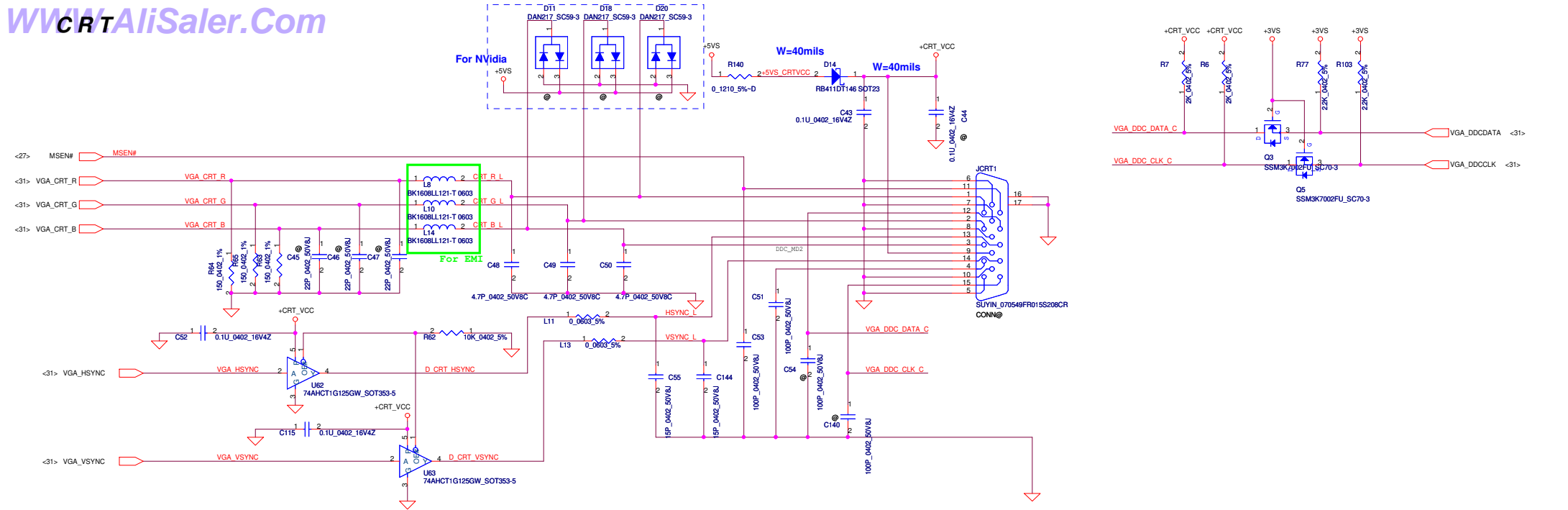
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



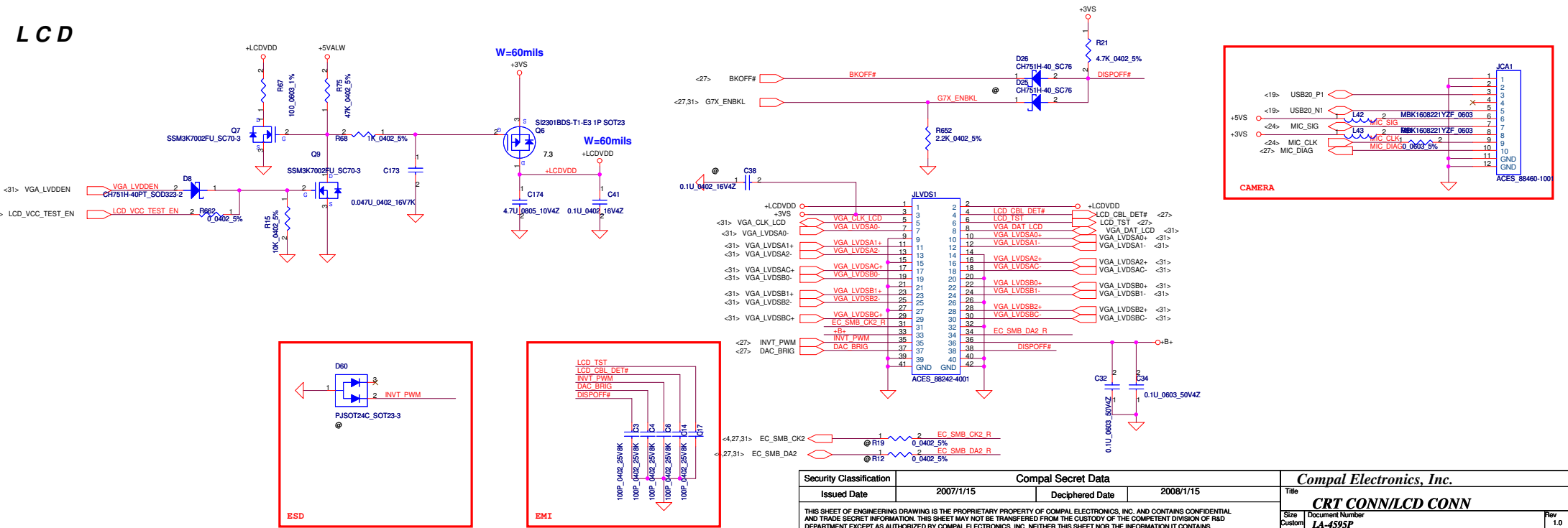
Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"



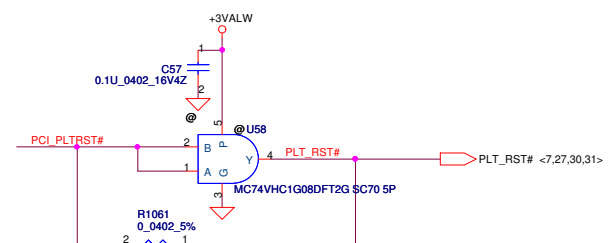
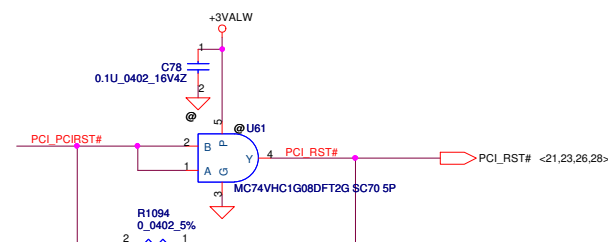
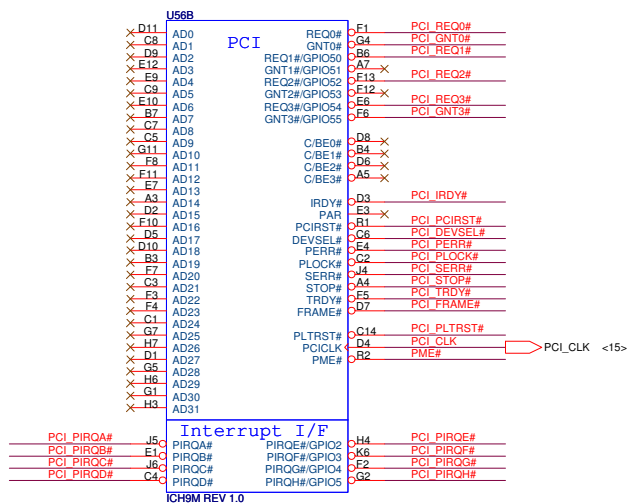
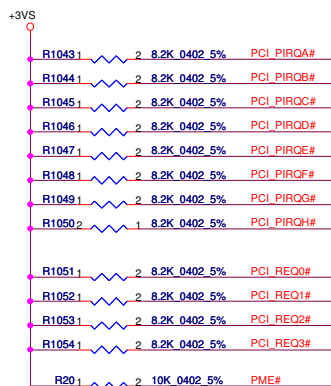
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DATE: 2007/1/15 DRAWN BY: [Signature] CHECKED BY: [Signature] APPROVED BY: [Signature]				Date:	Tuesday, February 17, 2009 Sheet 14 of 49



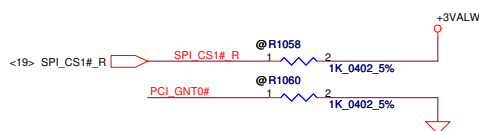
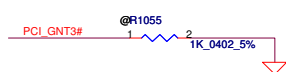
LCD



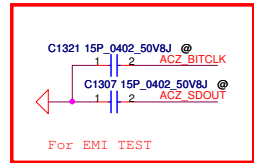
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	CRT CONN/LCD CONN
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Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

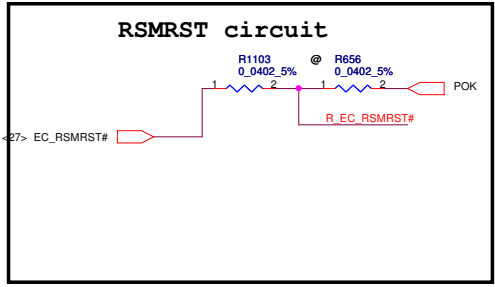


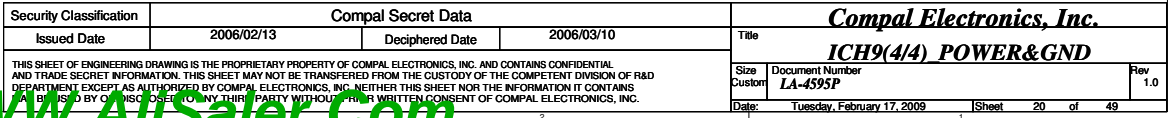
Security Classification		Compal Secret Data		Compal Electronics, Inc. ICH9(1/4)-PCI/INT	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	
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				Date:	Tuesday, February 17, 2009
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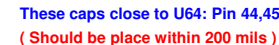


The schematic shows the ICH2 pin configuration. The ICH2 pin is connected to a 3V3 supply through a 1K_0402_5% resistor. The signal path is labeled ICH_RSVD, and the output is labeled ICH_RSVD <19>.

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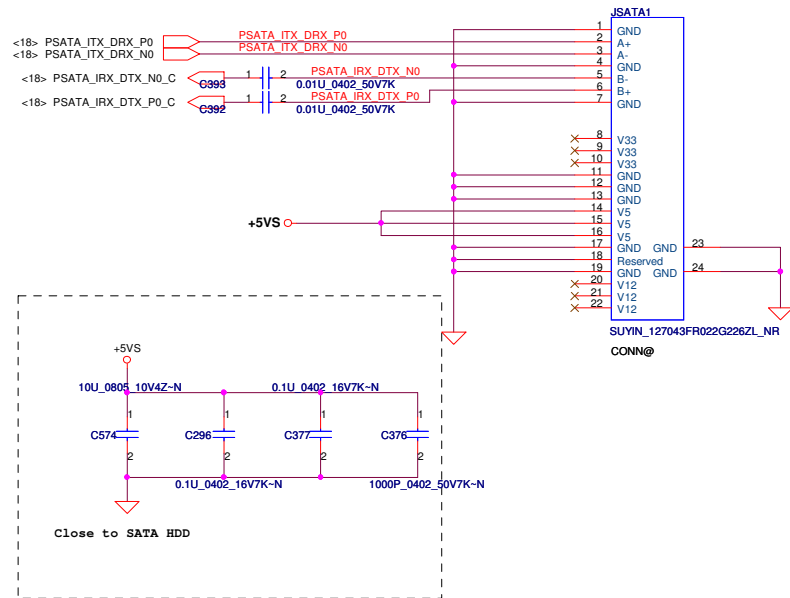


Compal Electronics, Inc.

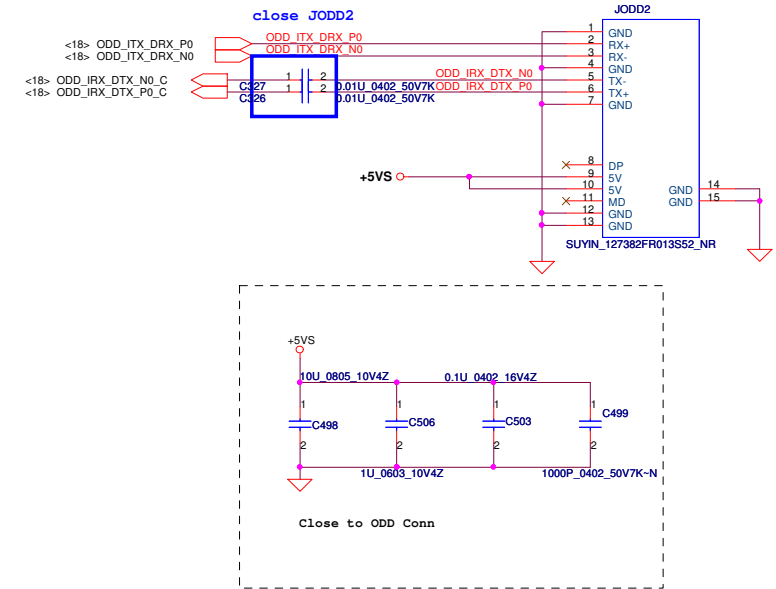
Gigabit LAN_RTL8111C

Size Custom Document Number **LA-4595P**

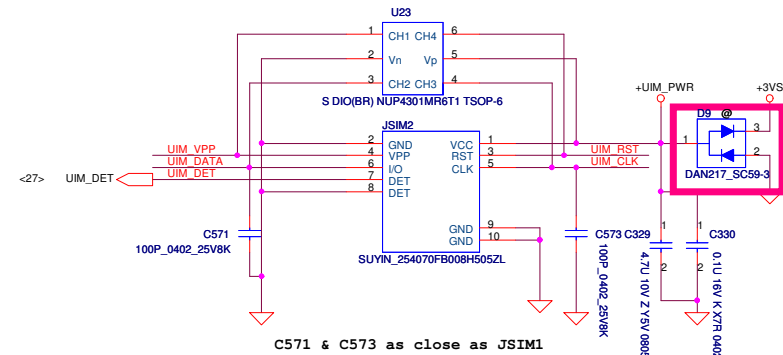
Date: Tuesday, February 17, 2009 Sheet 21 of 49



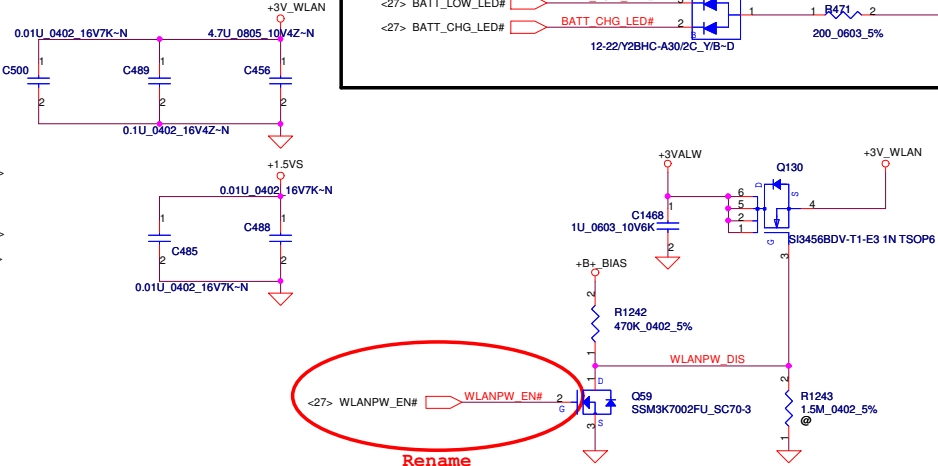
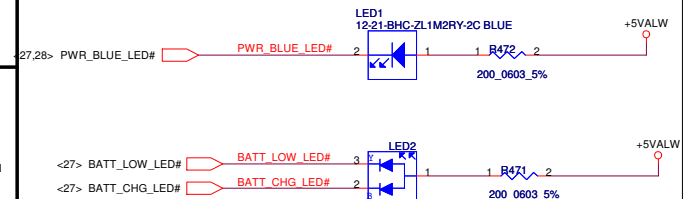
SATA ODD CONN



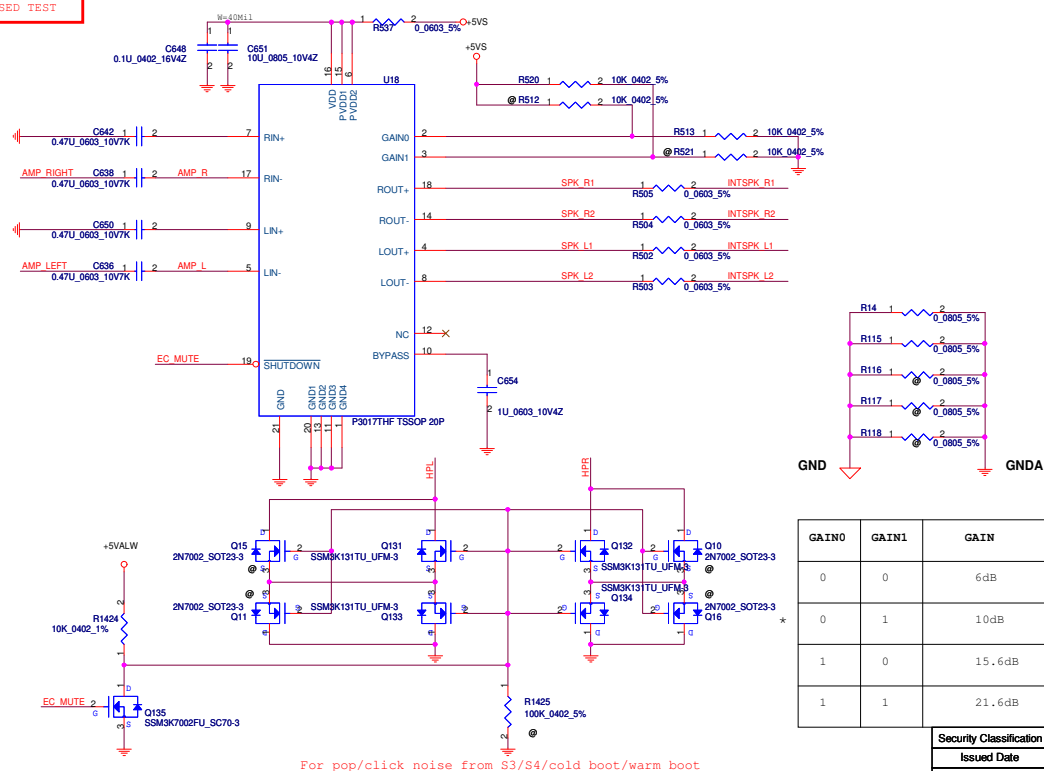
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Power status (Left)



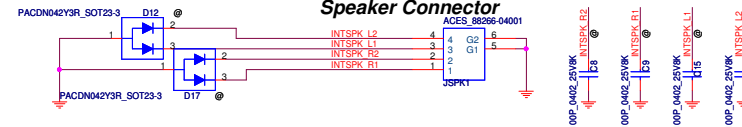
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GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

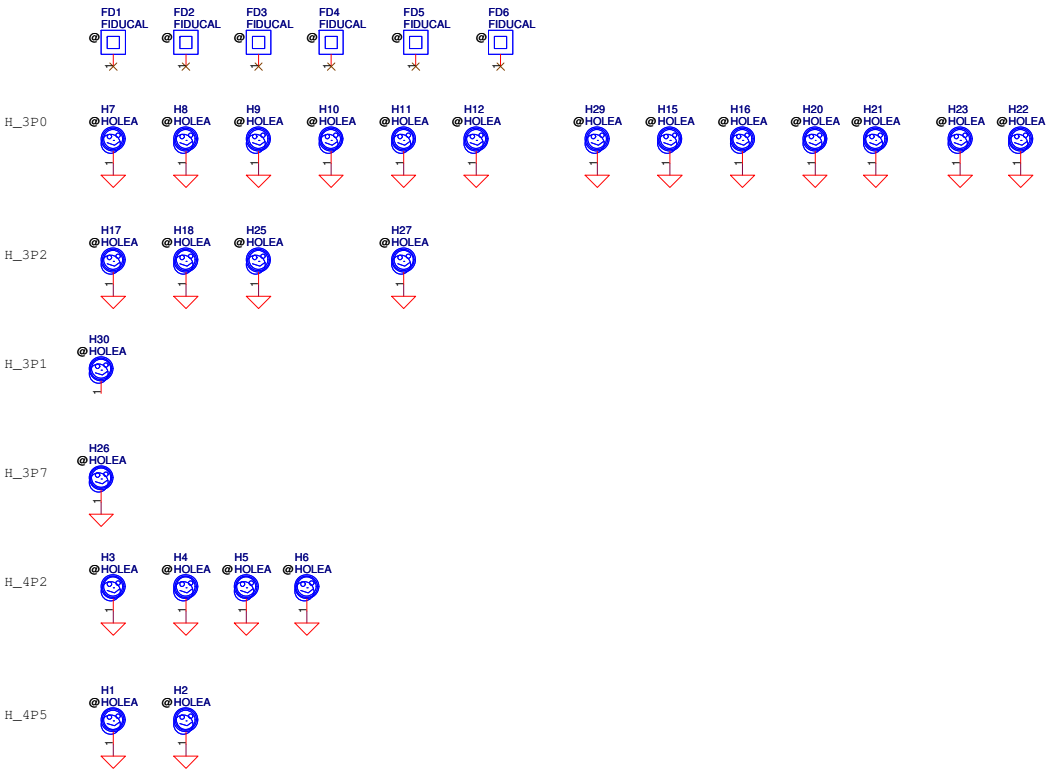
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

HEADPHONE OUT JACK

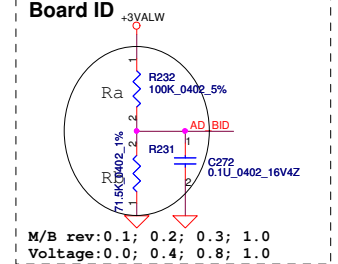


Compal Electronics, Inc.

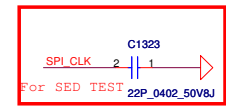
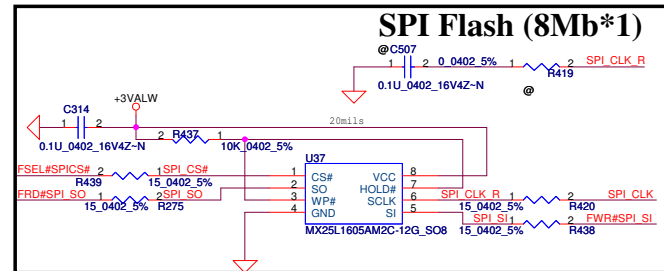
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			Size	Document Number
				LA-4595P



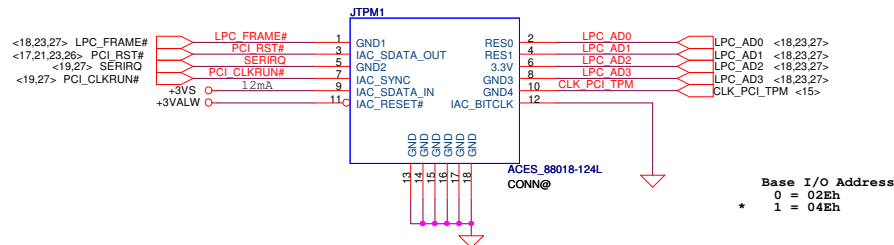
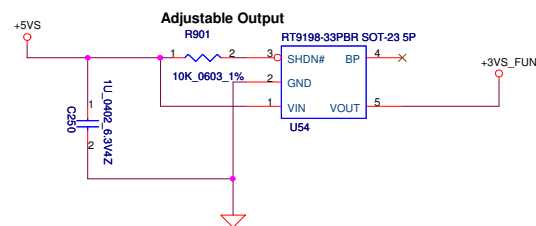
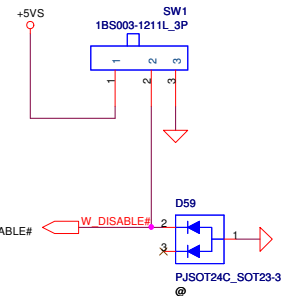
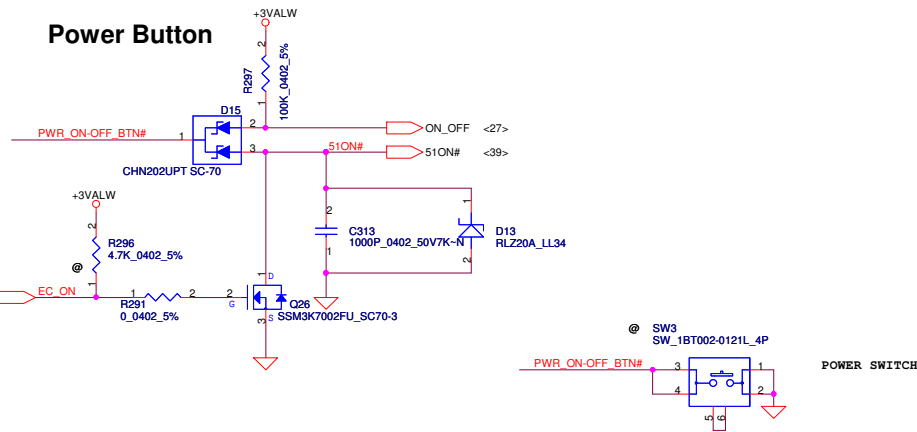
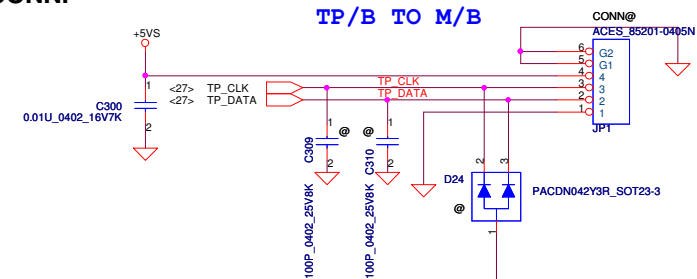
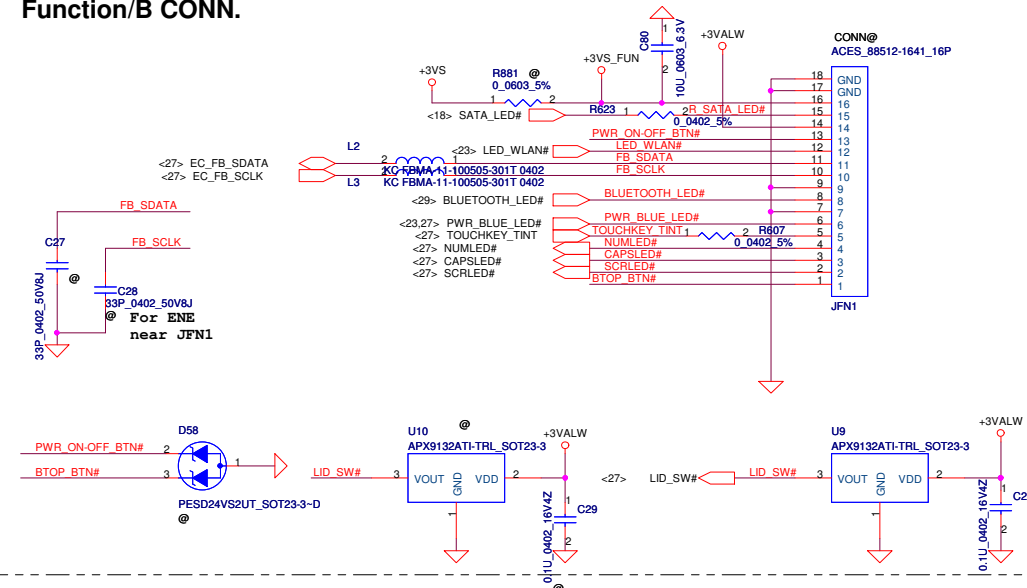
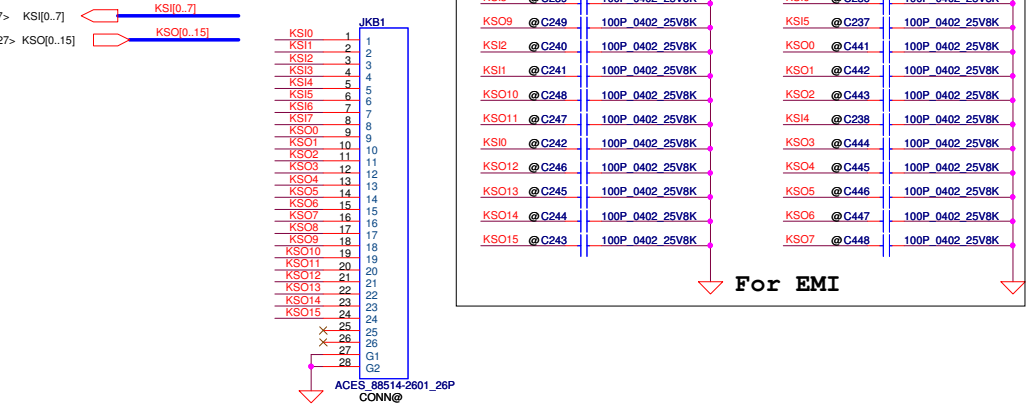
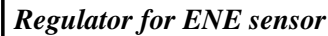
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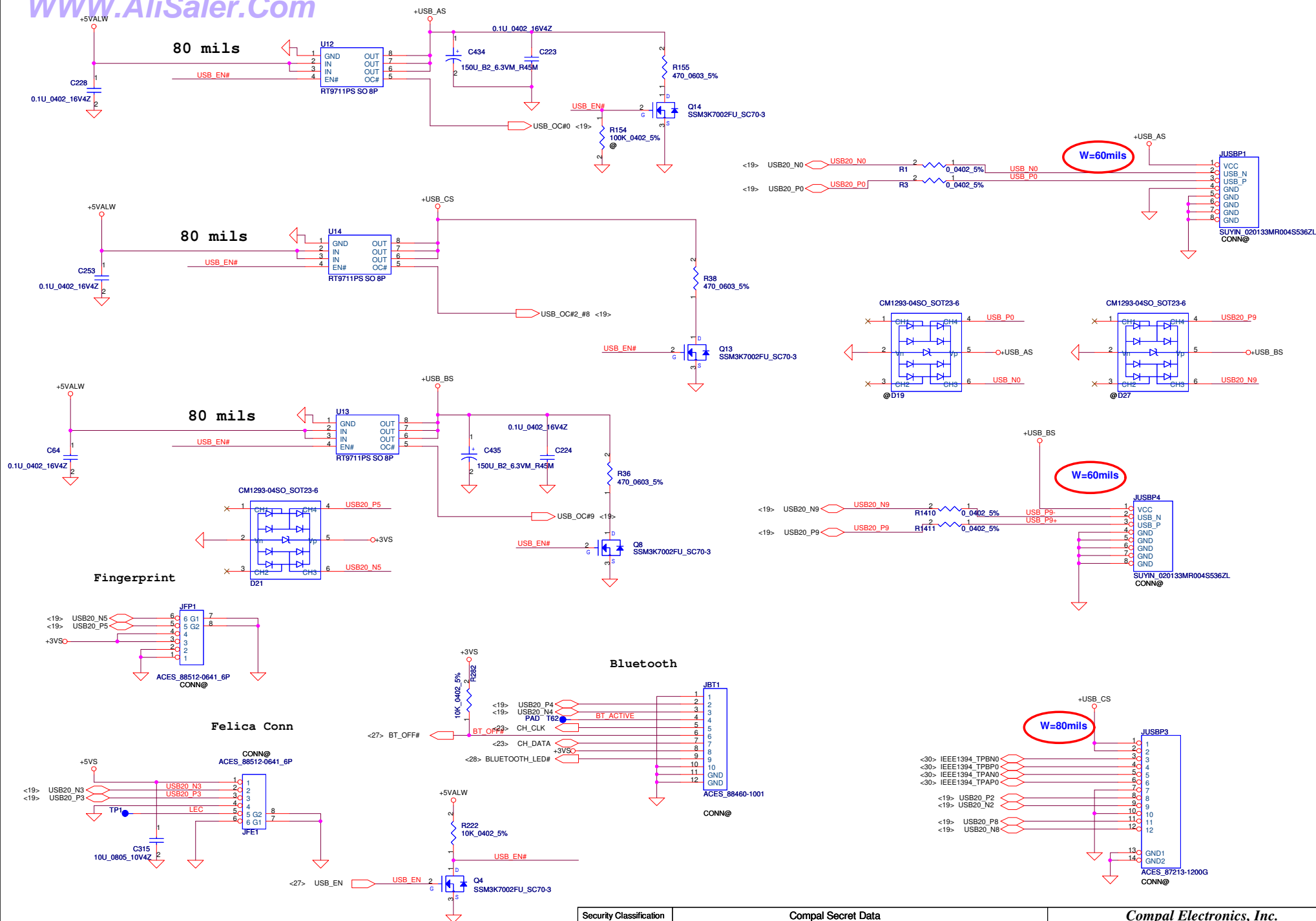
VCC	3.3V \pm 5%	0.6V - 1.6V
Ra	100k	
Board ID	Rb	
0	56.1K \pm 1%	0.683
1	34.8K \pm 1%	0.8519
2	48.4K \pm 1%	1.0459
3	56.2K \pm 1%	1.1873
4	71.5K \pm 1%	1.3758
5	91K \pm 1%	1.5723



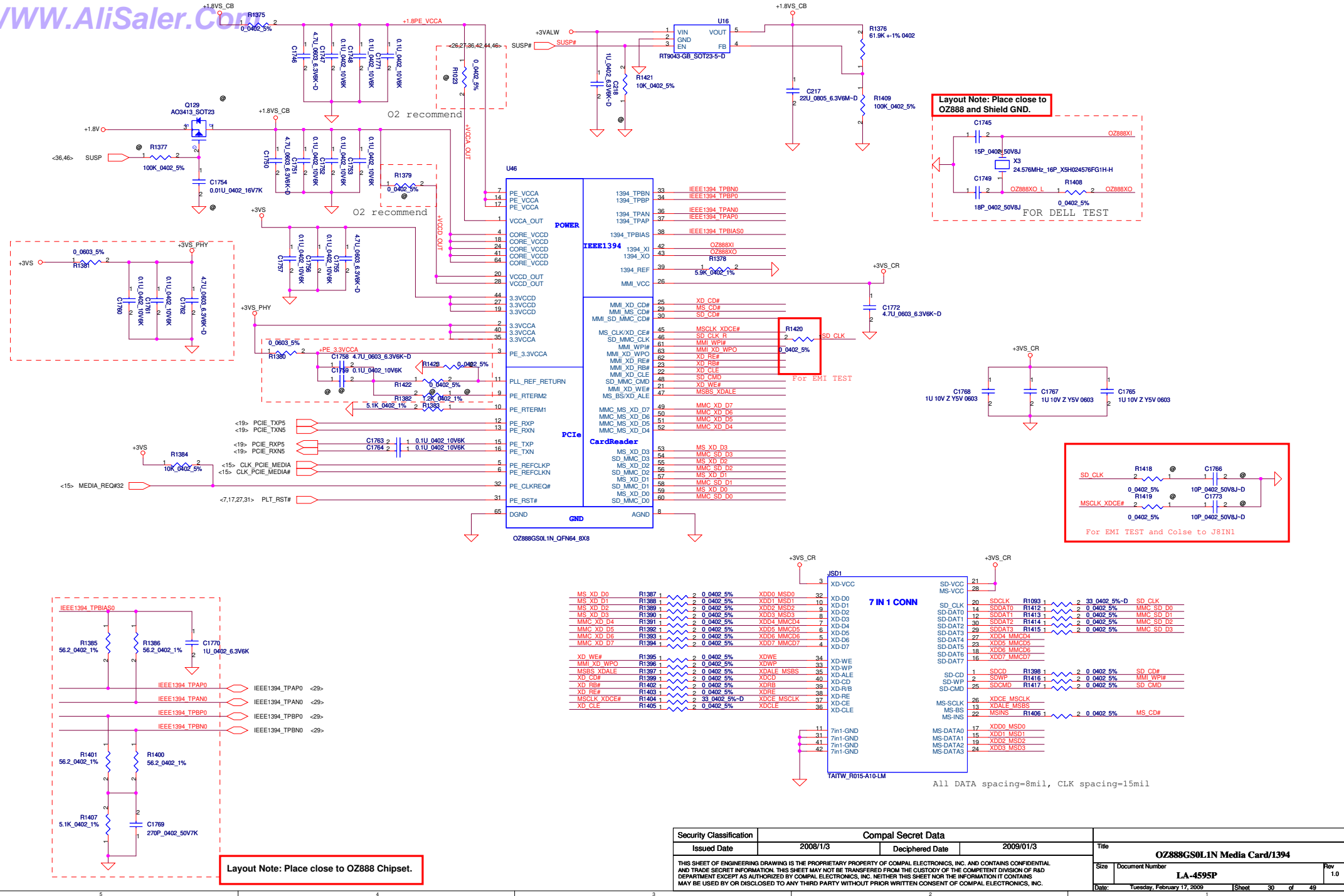
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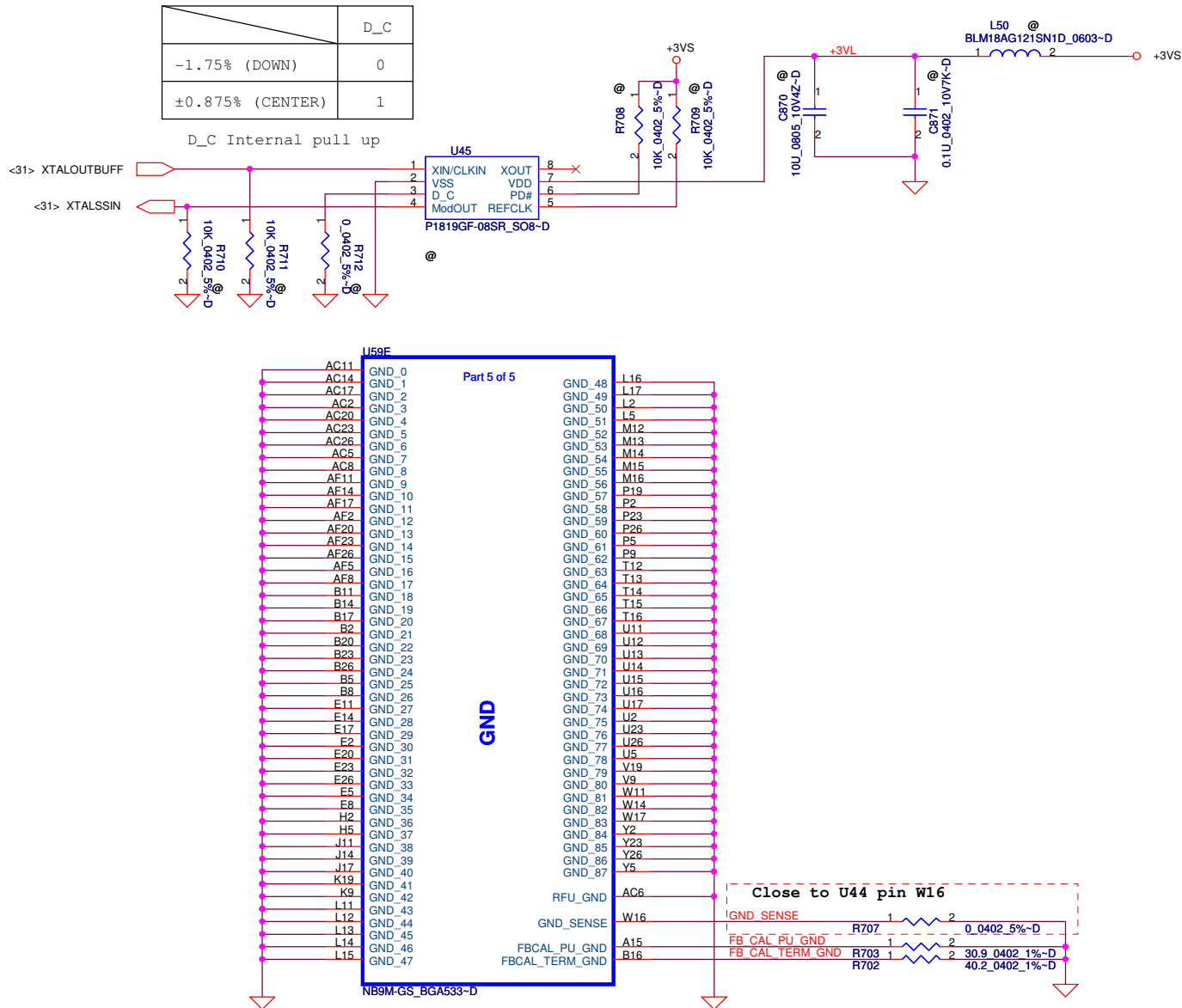
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				<p>USB/BlueTooth/FP/Felcia</p>	
				Size	Rev
Custom		Document Number	LA-4595P		1.0
Date:		Tuesday, February 17, 2009	Sheet	29	of 48







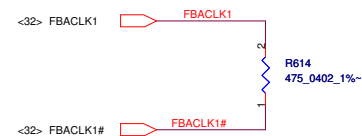
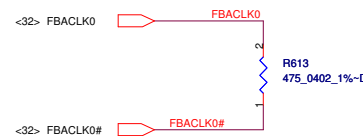
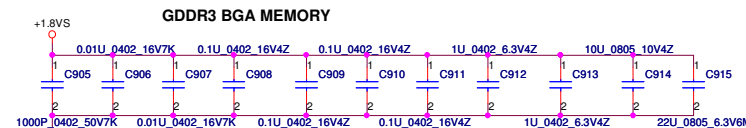
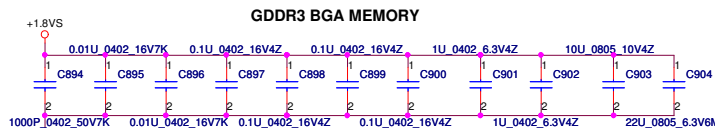
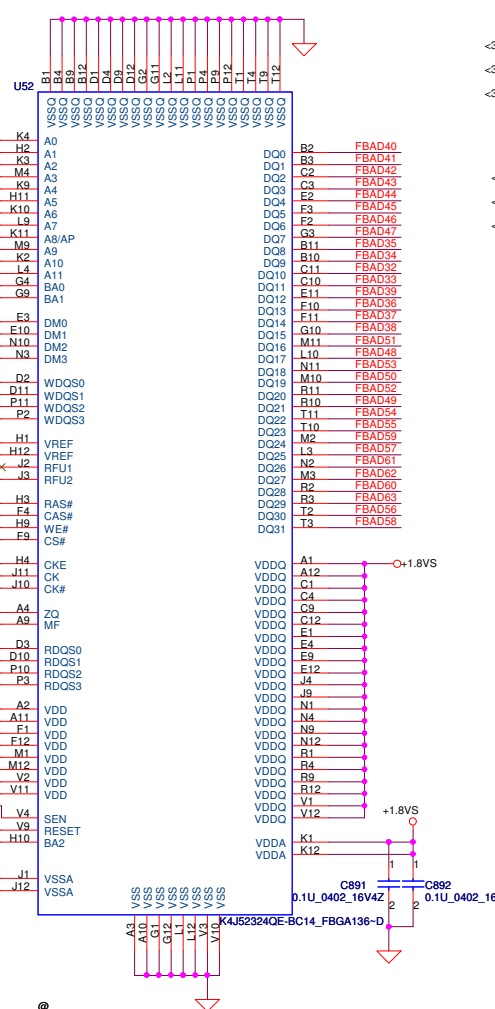
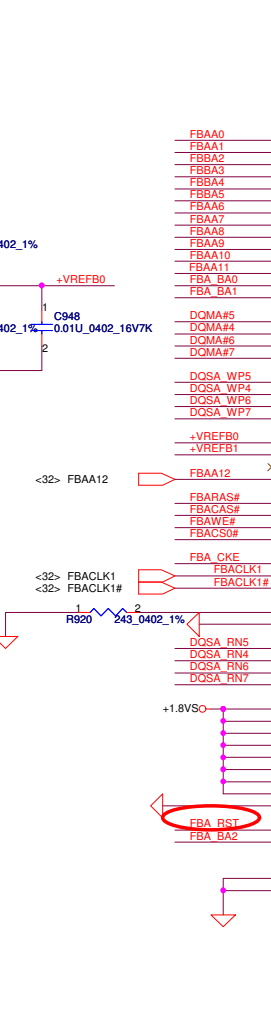
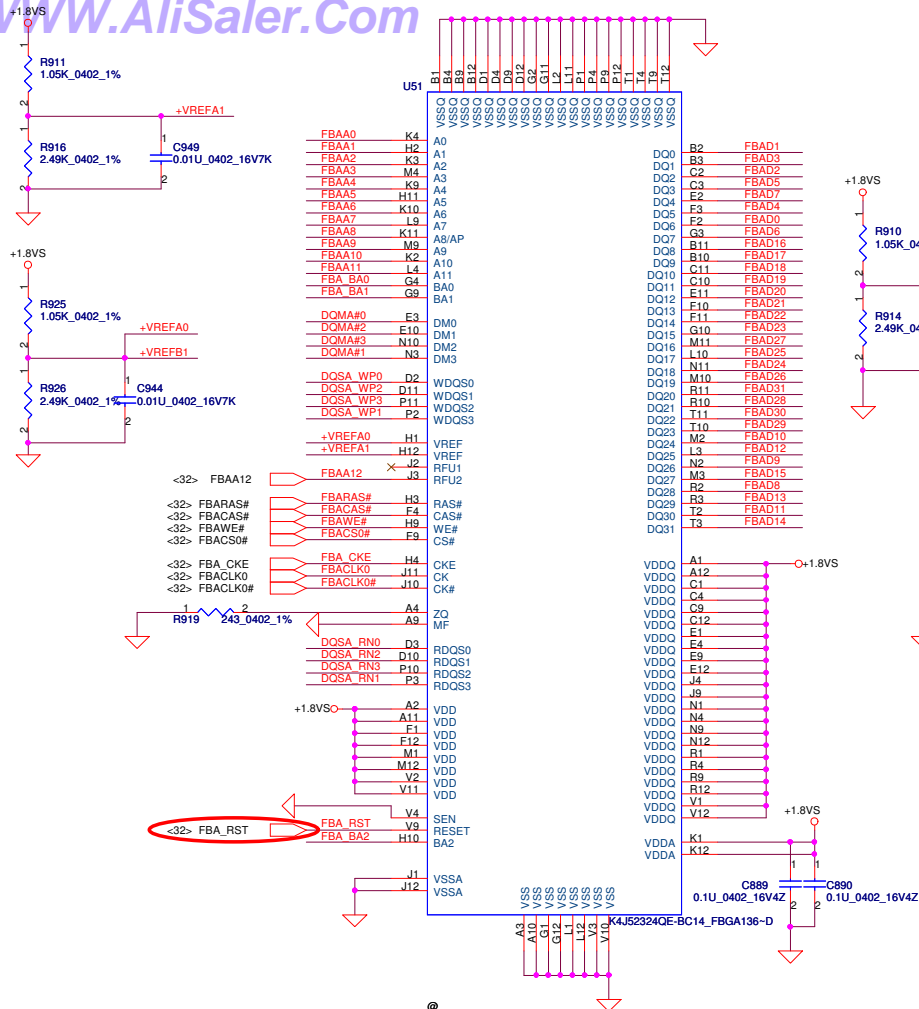
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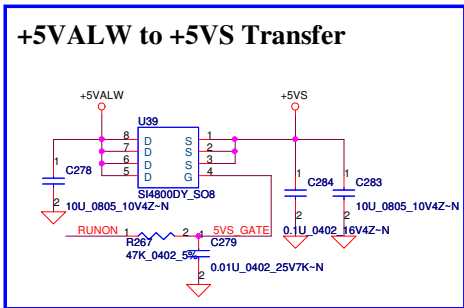
Compal Electronics, Inc.

Title		
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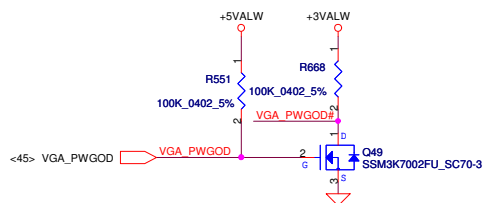
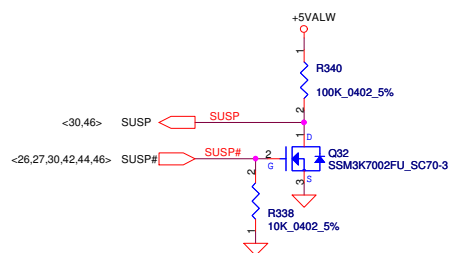
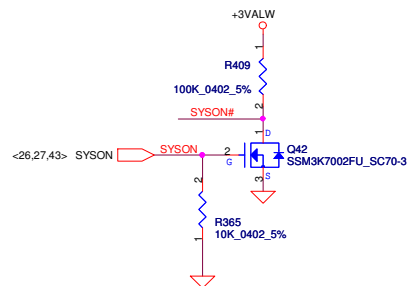
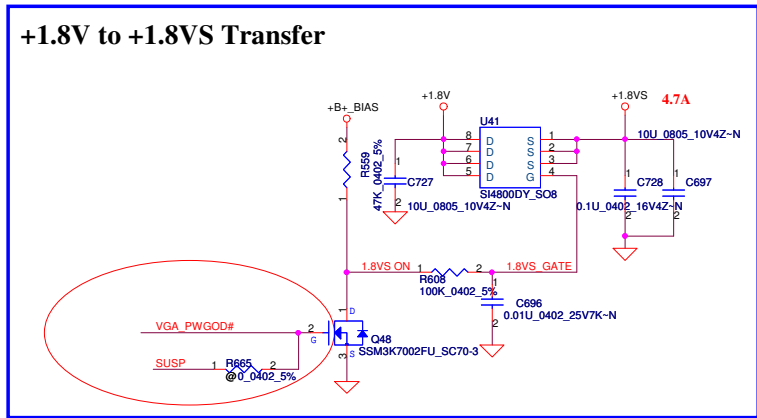


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+5VALW to +5VS Transfer

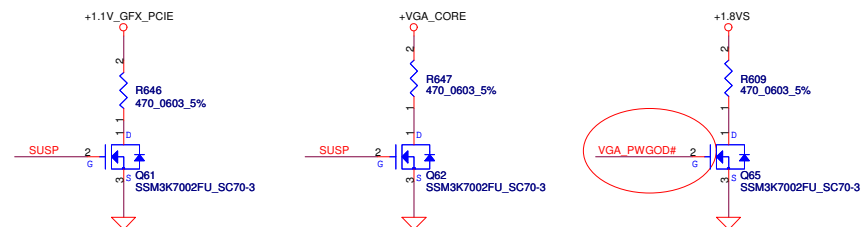


+1.8V to +1.8VS Transfer

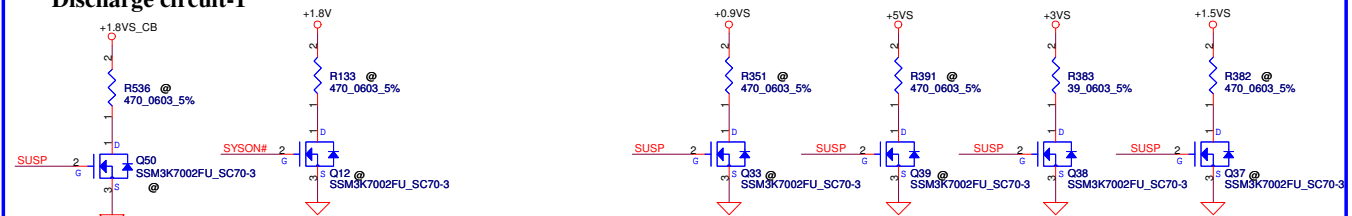


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

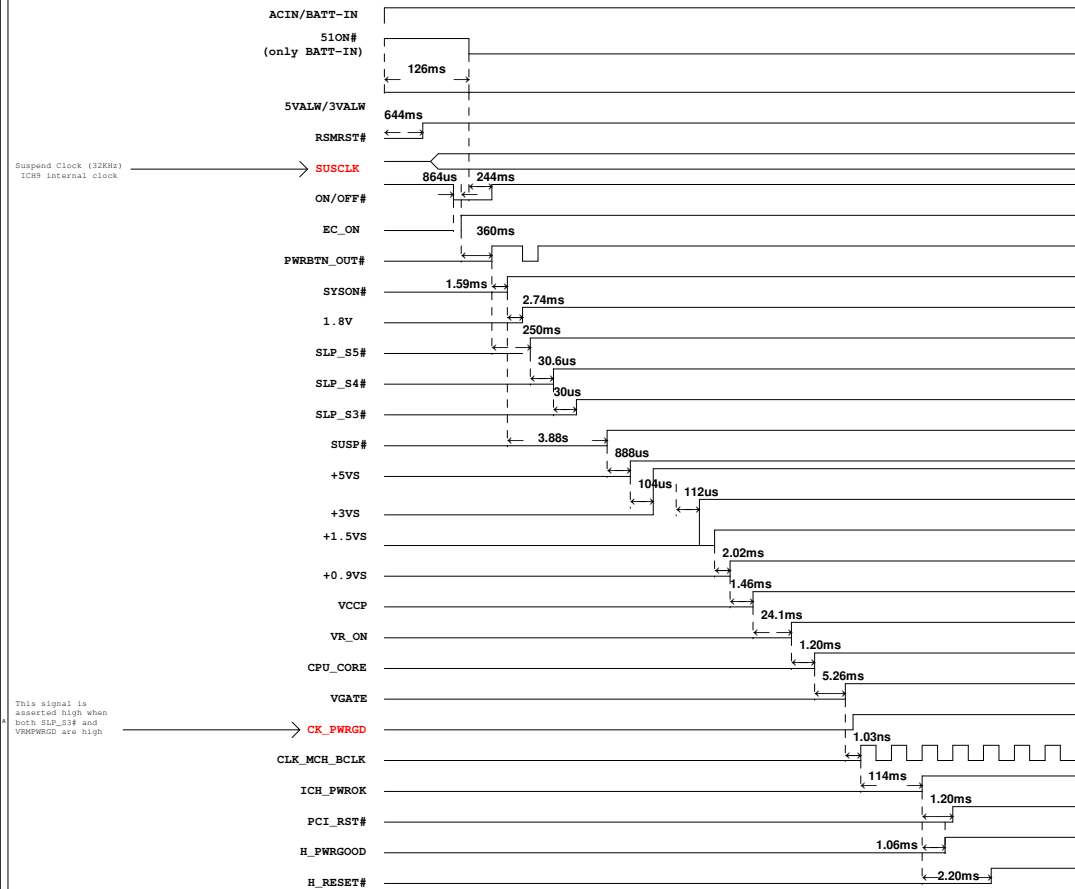
VGA Discharge circuit



Discharge circuit-1

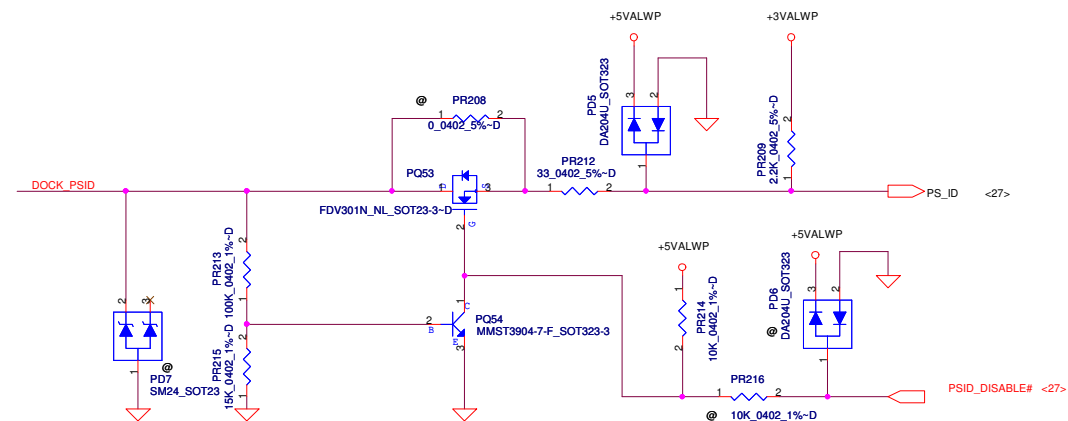
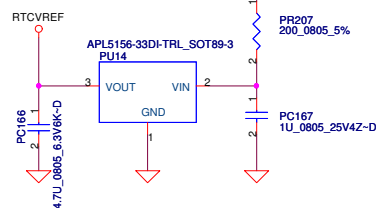
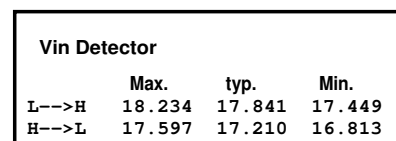
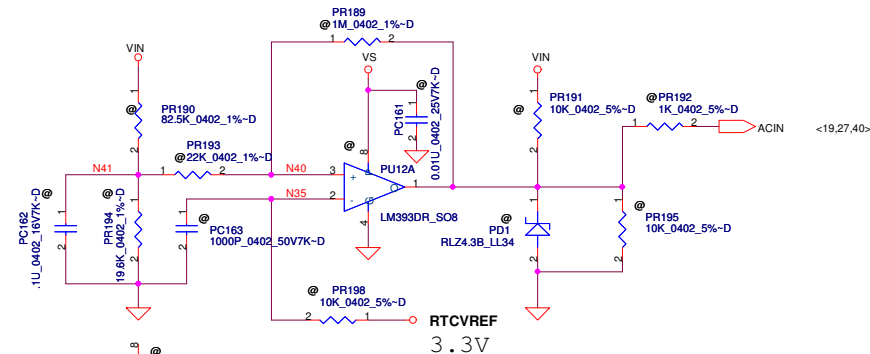


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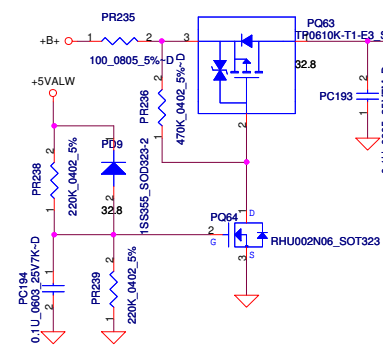
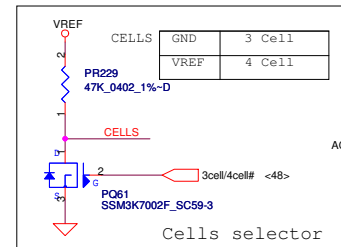
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1		Swap SW1	12/02	EE			
2		Update JUSBP3 pin define	12/02	EE			
3		R405 POP	12/02	EE			
4		U50 unPOP & R1190 POP	12/02	EE			
5		WWAN move to PORT6	12/02	BIOS			
6		Add C1391 & C1392	12/02	NVidia	LVDS single channel issue	Short U59.V2 & U59.V3. Add C1391 C1392 for IFPB_IOVDD	
7		Swap JSPK1 Pin	12/02	EE			
8		R101	12/04	EE	Change to 0805		
9		TPM Con	12/04	EE	Modify to Con		
10		R76 & R78 UnPOP	12/09	EE	EC update to Rev:C1		
11		Q7 & Q9	12/09	EE	Update Q7 & 9 footprint		
12		R658 & R281	12/11	EE	R685 UnPOP & R281 UnPOP for wake on LAN		
13		U89 & WLANPW_DIS#	12/11	EE	Add U89 for wake on LAN. Add WLANPW_DIS# of EC		
14		C1484 & C1485	12/11	EE	C1484 & C1485 modify to 1U form LAN vendor		
15		Update PW schematic	12/12	PW			
16		C260 & C252	12/15	EE	IDT ask UnPop		
17		Add D29 D28	12/15	ESD	ESD for LAN		
18		U9 Pop & U10 UnPop	12/15	ME			
19		Wake On WLAN	12/16	EE	Modify WLANPW_DIS# circuit		
20		Add T49 & T53	12/16	Layout			
21		C696	12/16	EE	Update PN		
22		WLANPW_DIS#	12/17	EE	Move WLANPW_DIS# to EC-GPIO40 and Del BTOP_ON		
23		L42 & L43	12/17	EMI	L42 & L43 update to Bead from 0 ohm		
24		C3 C4 C6 C14 C17	12/17	EMI	POP 100 P		
25		R69	12/17	EE	Update to Bead drom 100 ohm		
26		Cap	12/17	EMI	Add C1469 C1470 C1471 C1472 C1481 R81		
27		D21 D12 D17	12/17	ESD	ESD ask POP		
28		Update PW schematic	12/17	PW			
29		Update Q128 Q130 PN	12/18	EE			
30		Update Board ID	12/18	EE	R231		
31		Add U16 for OZ888	12/18	EE			
32		C1323 POP	12/18	EE	For Repart		
33		R1421 UnPOP	12/22	EE			
34		C292 C297	12/22	EE	Modify to 22P form 18P (Crystal Vendor)		
35		C1745 C1749	12/22	EE	Modify to 18P form 10P(C1749) and 15P from 10P(C1745)(Crystal Vendor)		
36		C1211	12/22	EE	Modify to 12P form 15P (Crystal Vendor)		
37		R1423 & R1422	01/07	EE	Add for O2		
38		L6 & R1190	01/10	EE	Change to 0805		
39		Modify LDO to +5VS	01/12	EE			
40		Add C80 & D59 & D60	01/12	EE			
41		Add components of JHP1	01/13	EE	For vendor		
42		R360 & R361	01/19	EE	Update R360 & R361 to 56 ohm		
43		U37	01/19	EE	Update U37 to SA00001KN10		
44		R231	01/19	EE	Update Board ID		

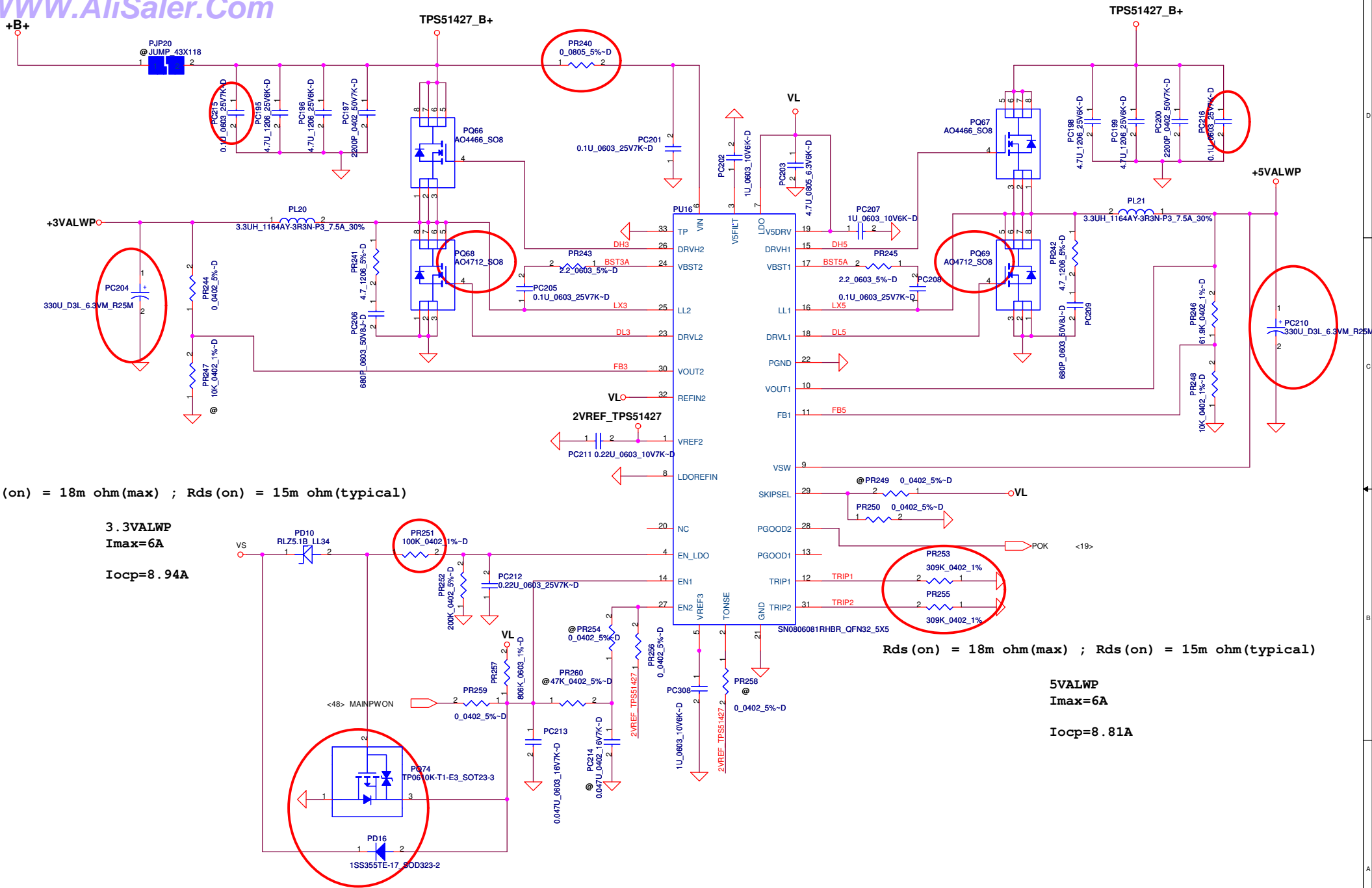
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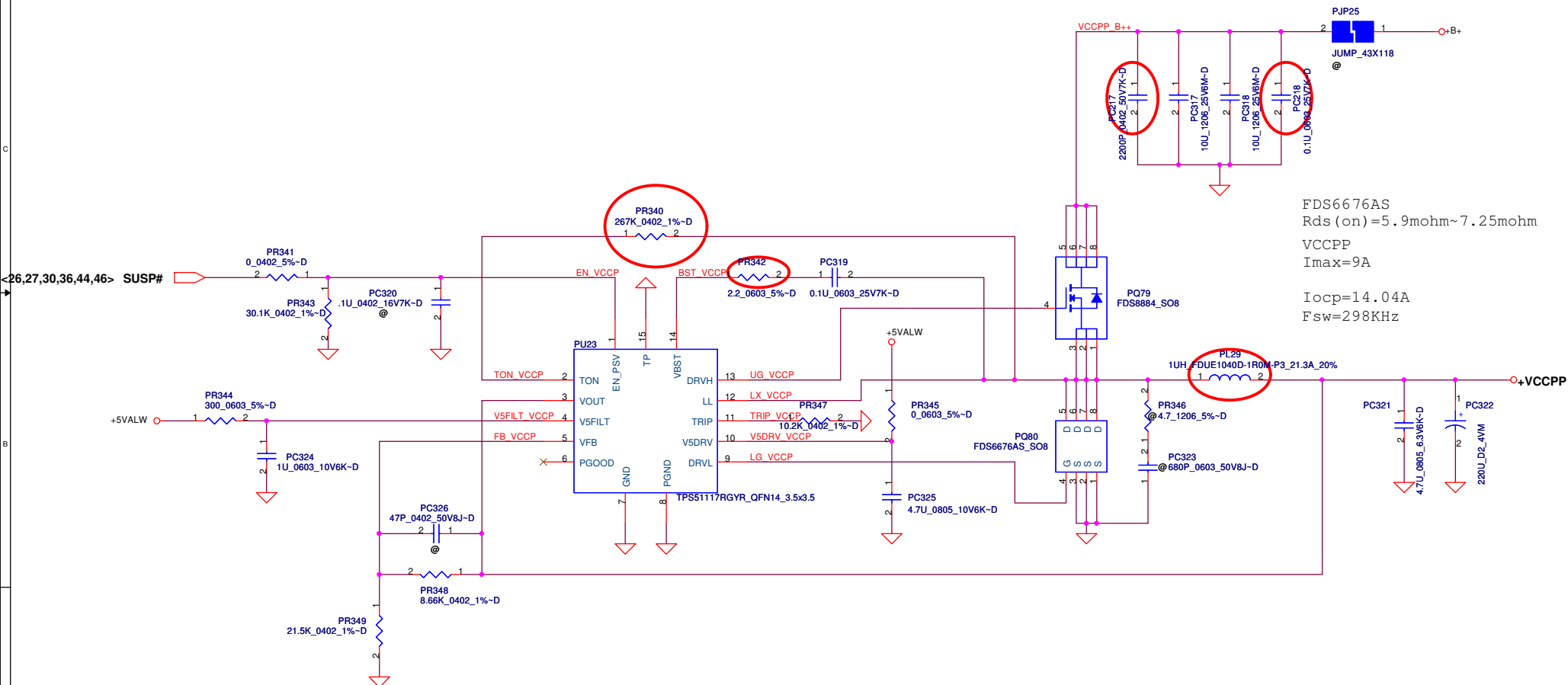
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Issued Date	2006/10/1	Deciphered Date	2007/5/01	DCIN / Vin Detector	
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90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR34) = 3.34A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz

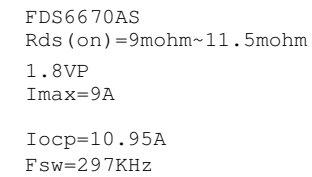




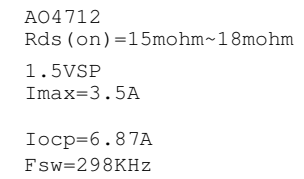
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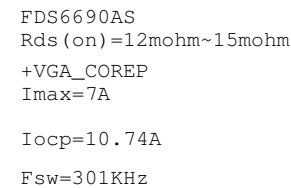
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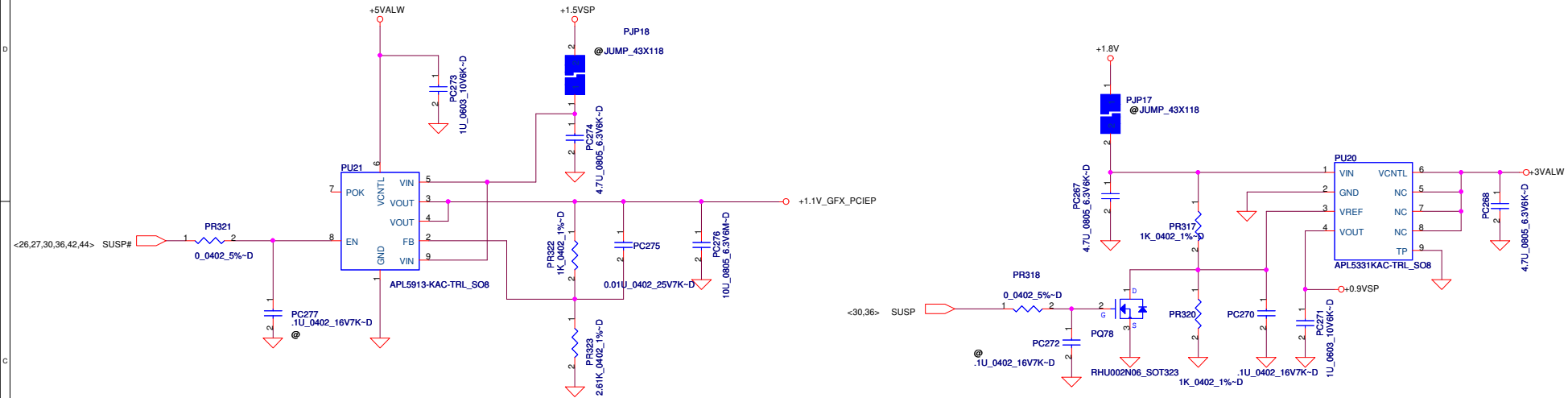
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	0.90V	1.09V	1.17V
GPU_VID_0	0	0	1
GPU_VID_1	0	1	1

output voltage adjustable network

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				+0.9VSP/+1.1V_GFX_PCIEP				
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				Date:				Tuesday, February 17, 2009

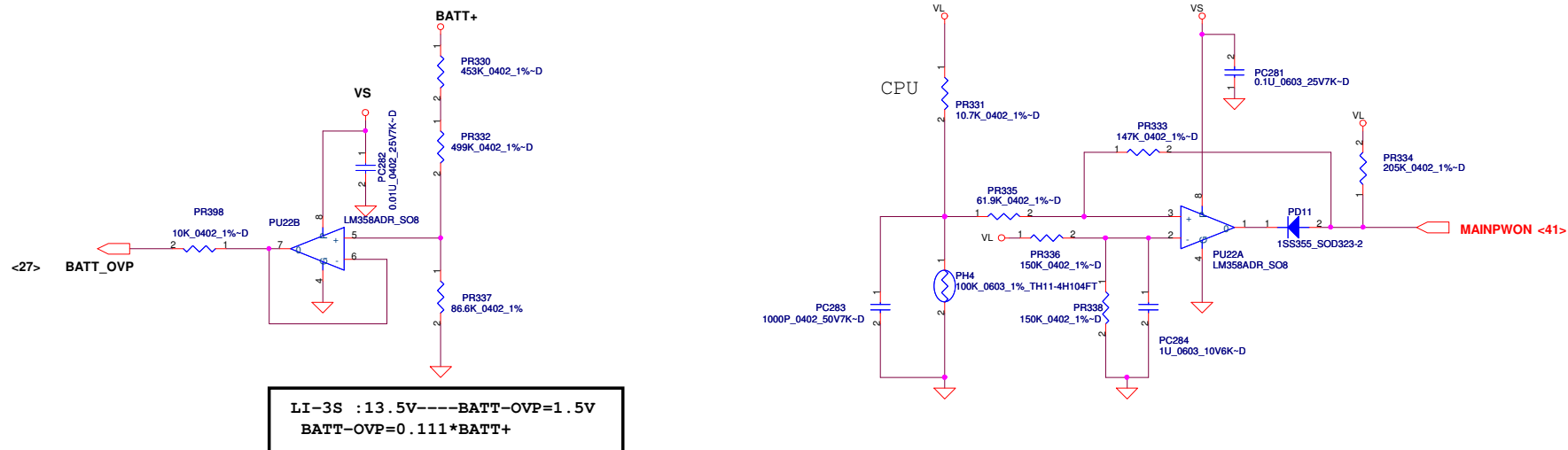


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PH1 under CPU botten side :
CPU thermal protection at 90 \pm 3 degree C
Recovery at 50 \pm 3 degree C



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						Size	Document Number		Rev 1.0
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	DCIN /Vin Detector	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
2			08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
3	40	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
4	48	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
5	39	DCIN /Vin Detector	08/12/12	COMPAL	increase capacitor for EMI request	add PC313 at 0.01uf and PC314 at 0.1uf	0.3
6	42	VCCPP	08/12/12	COMPAL	change resister for EMI request	change PR342 from 0 to 2.2	0.3
7	43	1.8VP	08/12/12	COMPAL	change resister for EMI request	change PR352 from 0 to 2.2	0.3
8	44	1.5VSP	08/12/12	COMPAL	change resister for EMI request	change PR362 from 0 to 2.2	0.3
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				Size	Document Number	Rev	
		LA-4595P	1.0				
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